

LCD_DATA[0..15]

LCD_DATA[0..15] [6]

- LCD_DATA0 7 I/O0
- LCD_DATA1 8 I/O1
- LCD_DATA2 9 I/O2
- LCD_DATA3 10 I/O3
- LCD_DATA4 13 I/O4
- LCD_DATA5 14 I/O5
- LCD_DATA6 15 I/O6
- LCD_DATA7 16 I/O7
- LCD_DATA8 29 I/O8
- LCD_DATA9 30 I/O9
- LCD_DATA10 31 I/O10
- LCD_DATA11 32 I/O11
- LCD_DATA12 35 I/O12
- LCD_DATA13 36 I/O13
- LCD_DATA14 37 I/O14
- LCD_DATA15 38 I/O15

- A1 5 A0
- A2 4 A1
- A3 3 A2
- A4 2 A3
- A5 1 A4
- A6 44 A5
- A7 43 A6
- A8 42 A7
- A9 27 A8
- A10 26 A9
- A11 25 A10
- A12 24 A11
- A13 22 A12
- A14 21 A13
- A15 20 A14
- A16 19 A15
- A17 18 A16
- A18 23 A17
- A19 28 A18

PSRAM

PSRAM, 512KX15, DNL

WE 17

CSn 6

OE 41

UB 40

LB 39

VDD 11

VDD 33

GND 12

GND 34

3V3

0.1UF,DNL

3V3

4.7K_NWK4,DNL

4.7K

4.7K,DNL

SRAM_WEn

SRAM_CSn

SRAM_OEn

SRAM_BHEn

SRAM_BLEn

R9 LOADED TO TELL MCU TO USE SDRAM

LOAD EITHER U2 OR U4 (NOT BOTH) DEFAULT IS SDRAM (U4)

SDRAM

SDRAM, 1MX16 TSOP50

CLK 35

CKE 34

A0 21

A1 22

A2 23

A3 24

A4 27

A5 28

A6 29

A7 30

A8 31

A9 32

A10 20

A11 19

CSn 18

WE 15

RASn 17

CASn 16

LDQM 14

UDQM 36

DQ0 2

DQ1 3

DQ2 5

DQ3 6

DQ4 8

DQ5 9

DQ6 11

DQ7 12

DQ8 39

DQ9 40

DQ10 42

DQ11 43

DQ12 45

DQ13 46

DQ14 48

DQ15 49

3V3

0.1UF

3V3

0.1UF

3V3

10UF,6.3V

3V3

0.1UF

3V3

10UF,6.3V

3V3

0.1UF

3V3

10UF,6.3V

SRAM_OEn

SRAM_WEn

SRAM_BHEn

SDRAM_WEn

SDRAM_CASn

SDRAM_RASn

SDRAM_CLK

SDRAM_CKE

SDRAM_DQM0

SDRAM_DQM1

SDRAM_CSn

ENET_MDIO [5]

ENET_MDC [5]

YDRIVE [6]

ENET_RXD1 [5]

ENET_RXD0 [5]

ENET_REFCLK [5]

ENET_RX_ER [5]

SRAM_CSn

ENET_MDIO [5]

ENET_MDC [5]

YDRIVE [6]

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ENET_RXD0 [5]

ENET_REFCLK [5]

ENET_RX_ER [5]

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SDRAM_RASn

SDRAM_CLK

SDRAM_CKE

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SDRAM_DQM1

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ENET_REFCLK [5]

ENET_RX_ER [5]

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SDRAM_RASn

SDRAM_CLK

SDRAM_CKE

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SDRAM_DQM1

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ENET_MDC [5]

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ENET_RXD0 [5]

ENET_REFCLK [5]

ENET_RX_ER [5]

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SDRAM_WEn

SDRAM_RASn

SDRAM_CLK

SDRAM_CKE

SDRAM_DQM0

SDRAM_DQM1

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ENET_MDC [5]

YDRIVE [6]

ENET_RXD1 [5]

ENET_RXD0 [5]

ENET_REFCLK [5]

ENET_RX_ER [5]

SDRAM_CSn

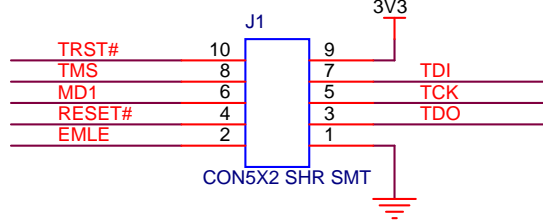
SDRAM_WEn

SDRAM_RASn

SDRAM_CLK

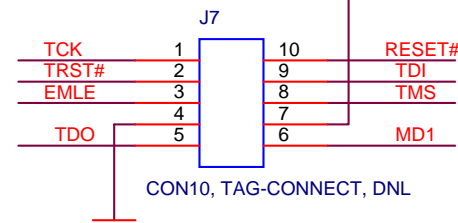
SDRAM_CKE

JTAG

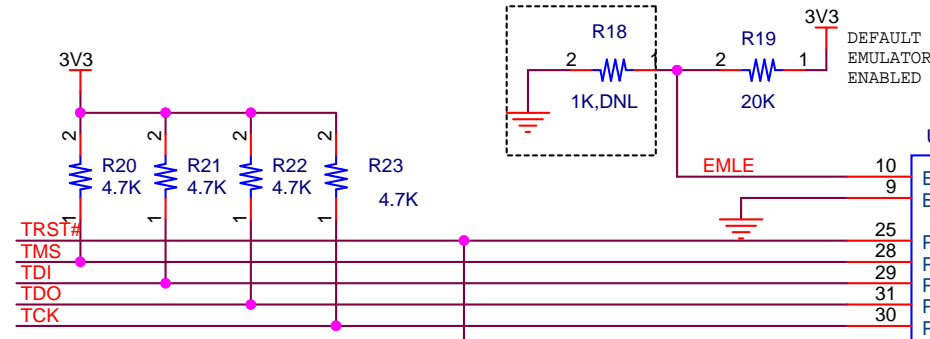


FDI MINI-JTAG INTERFACE

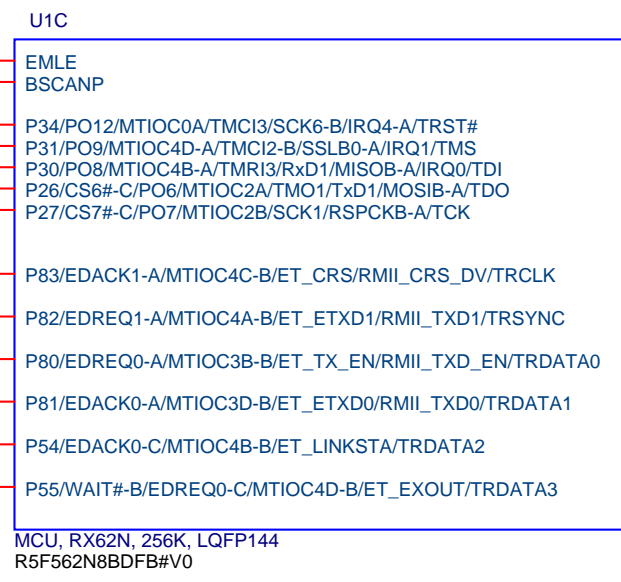
REV 2



TAG-CONNECT TC2050-IDC-NL



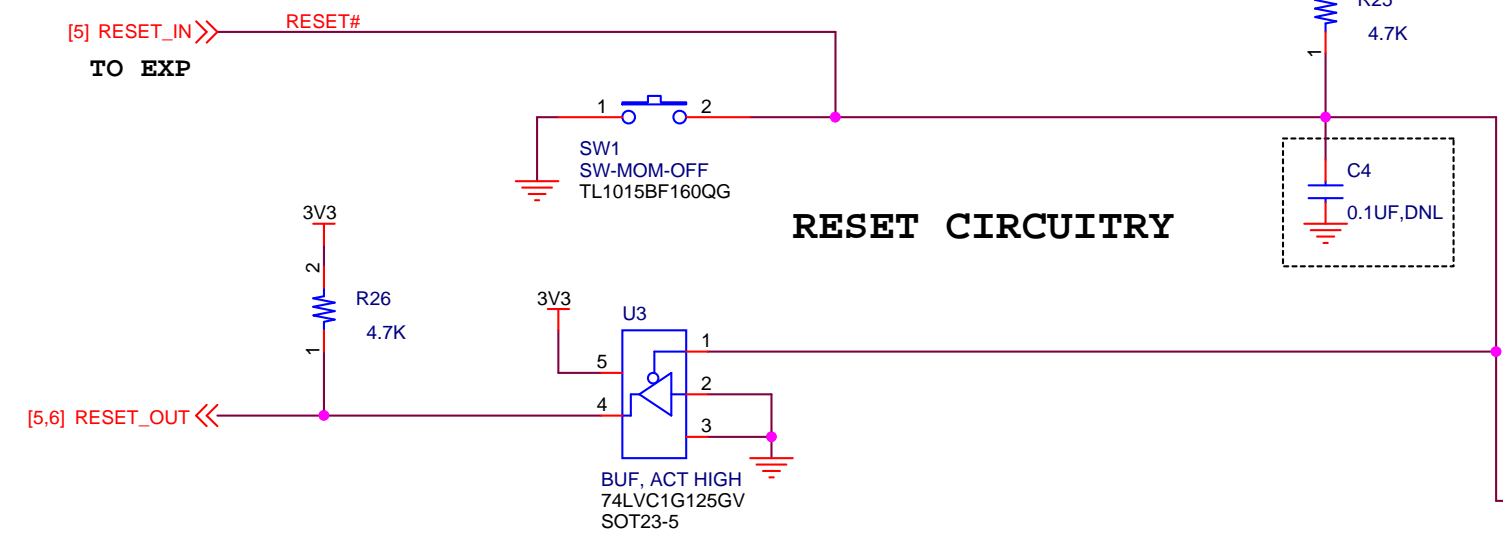
REV 2 - JTAG NO LONGER GOES TO EXP CONN



RX MCU JTAG/DMA

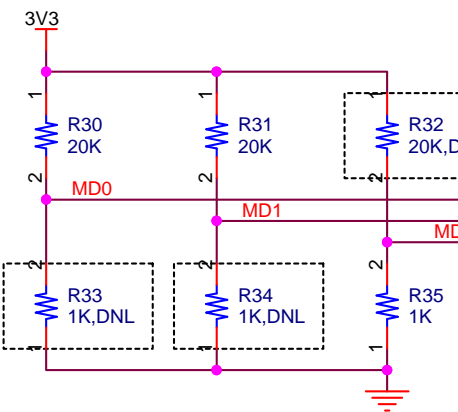
MCU, RX62N, 256K, LQFP144
R5F562N8BDFB#V0

RESET CIRCUITRY



RX MCU CLOCK/RST/CFG

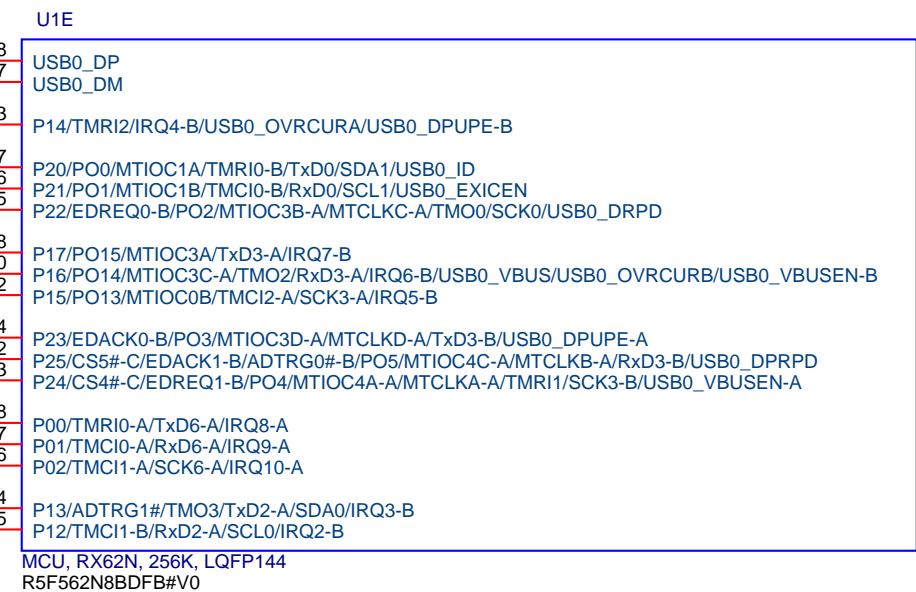
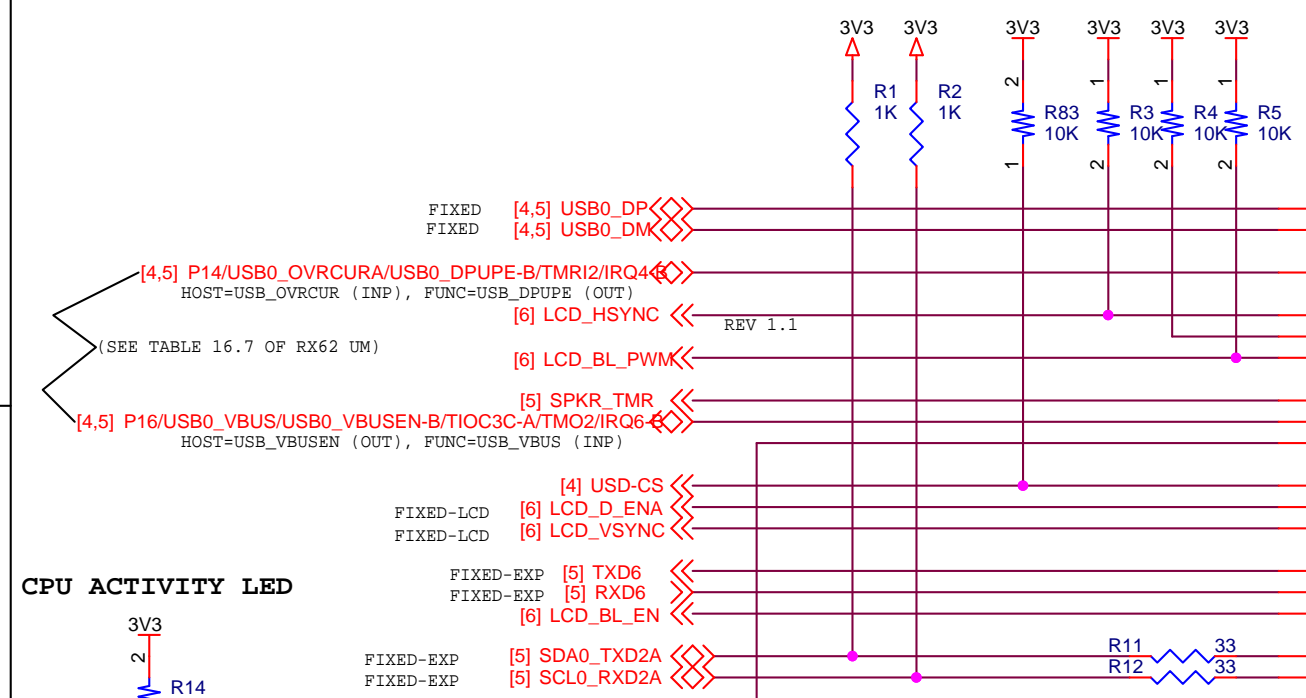
REV 2 - MCU CONFIG NO LONGER GOES TO EXP CONN



MD0=1, MD1=1 FOR SINGLE CHIP MODE (DEFAULT)
 MD0=1, MD1=0 FOR SCI BOOT MODE
 MD0=0, MD1=1 FOR USB BOOT MODE

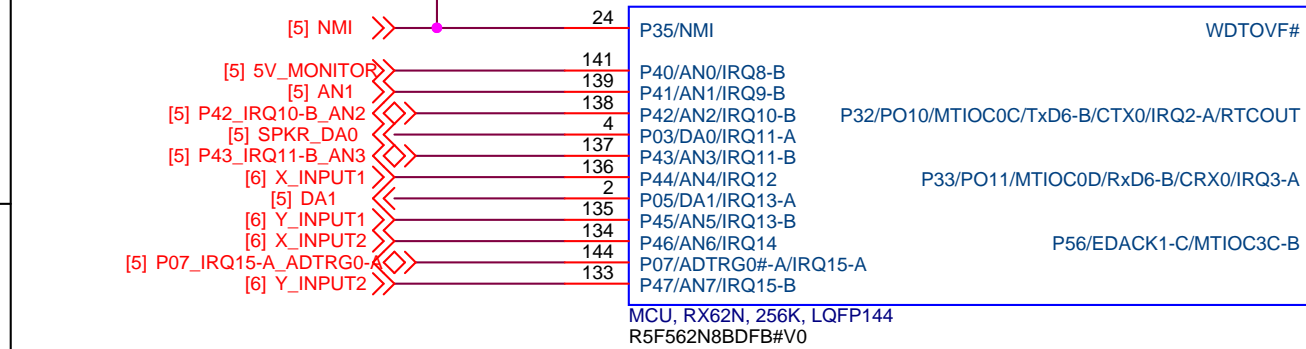
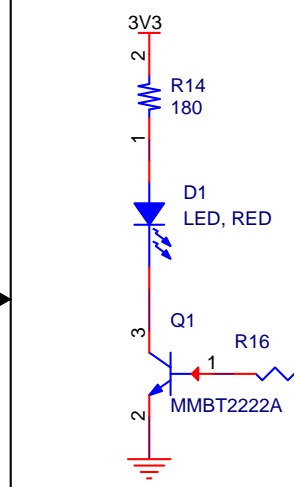
MDE=0 FOR LITTLE ENDIAN

FUTURE DESIGNS, INC. 2702 TRIANA BLVD HUNTSVILLE, AL 35805		FDI
Title uEZGUI-RX 3.5"		
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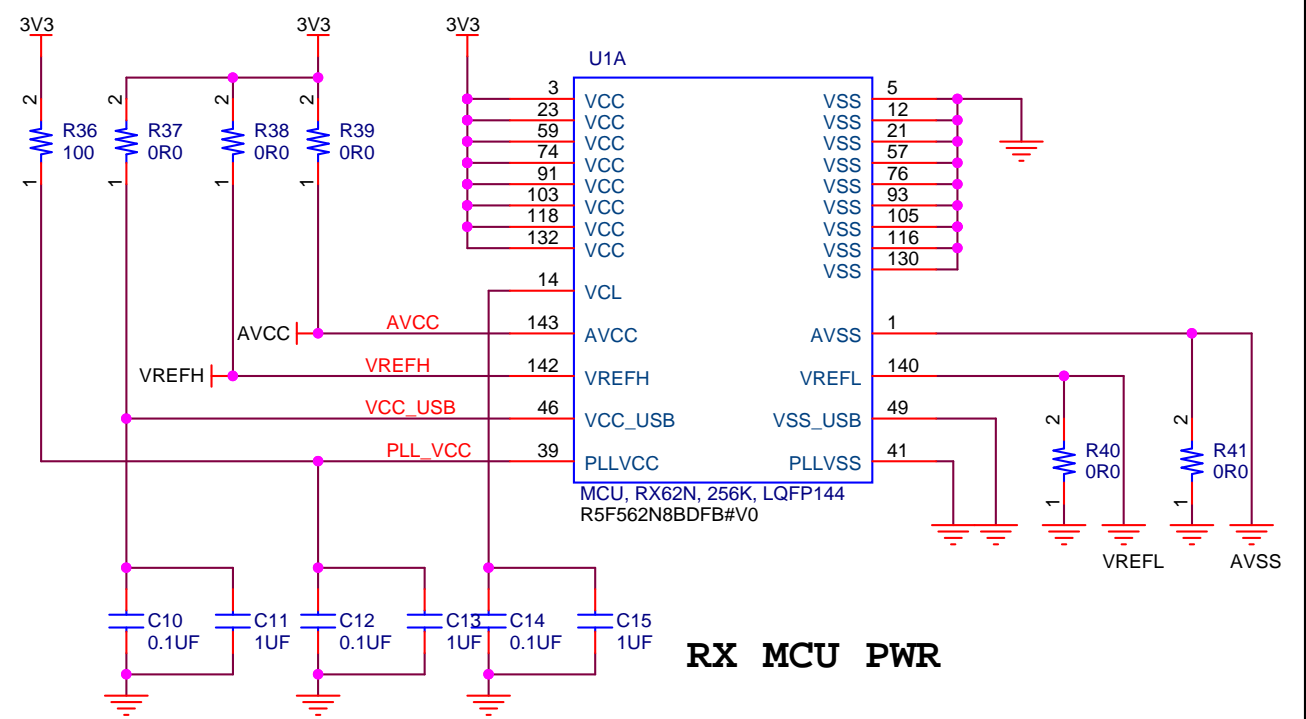


RX MCU SERIAL/IRQ/TMR

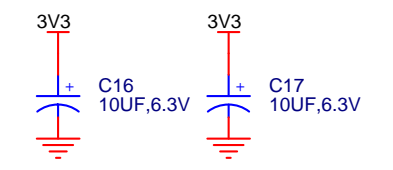
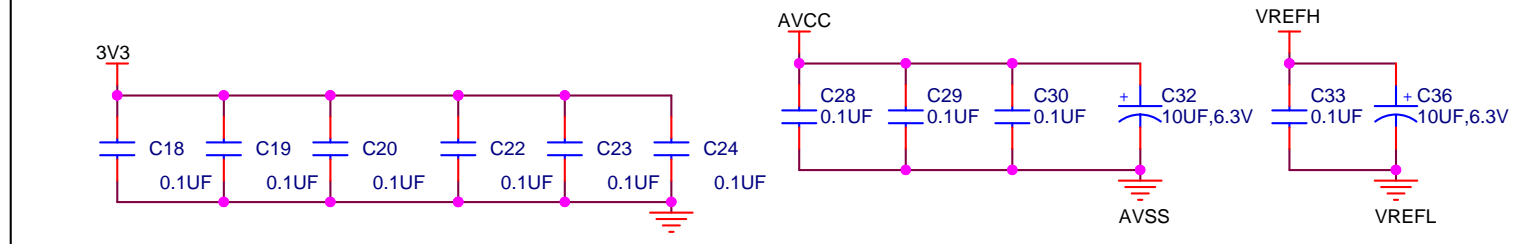
CPU ACTIVITY LED



RX MCU ANALOG



RX MCU PWR



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[3,5] P16/USB0_VBUS/USB0_VBUSEN-B/TIOC3C-A/TMO2/IRQ6-B

HOST=USB_VBUSEN (OUT), FUNC=USB_VBUS (INP)

[3,5] P14/USB0_OVRCURA/USB0_DPUPE-B/TMRI2/IRQ4-B

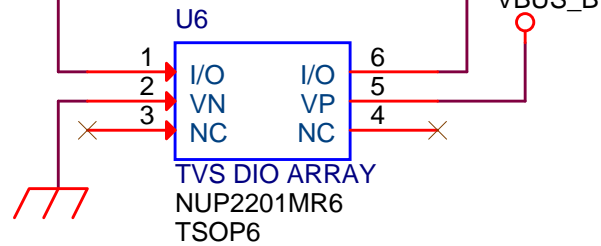
HOST=USB_OVRCUR (INP), FUNC=USB_DPUPE (OUT)

NOTE: THESE COMPONENTS MAY INTERFERE WITH HOST MODE OPERATION ON AN EXPANSION BOARD

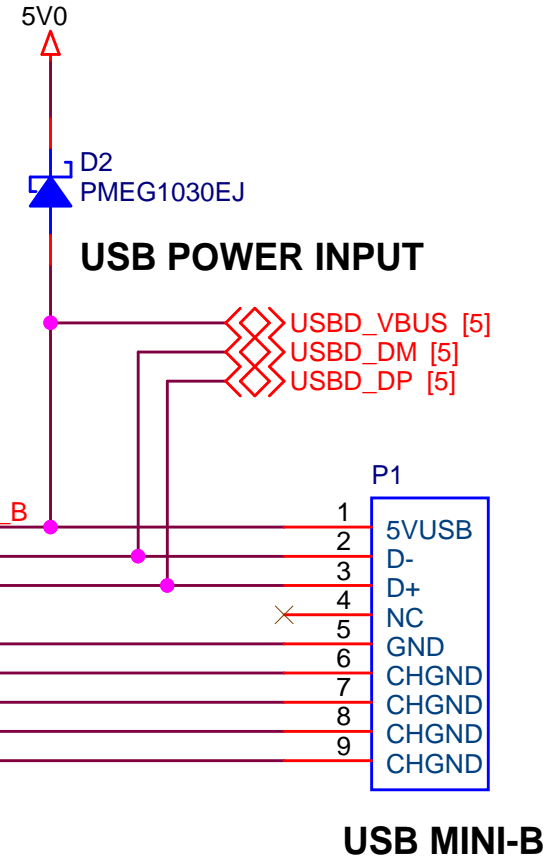
[3,5] USB0_DM

[3,5] USB0_DP

USB PROTECTION



USB DEVICE (FUNCTION)

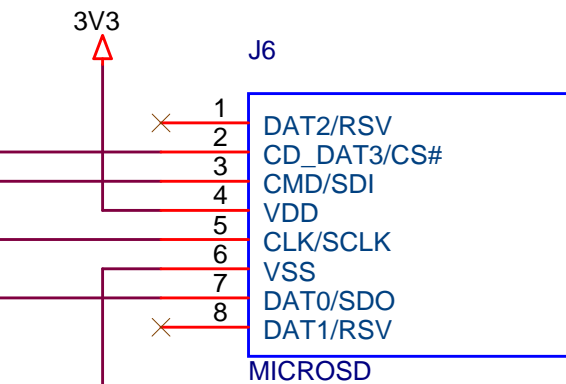


[3] USD-CS

[1,5,6] MOSI-A

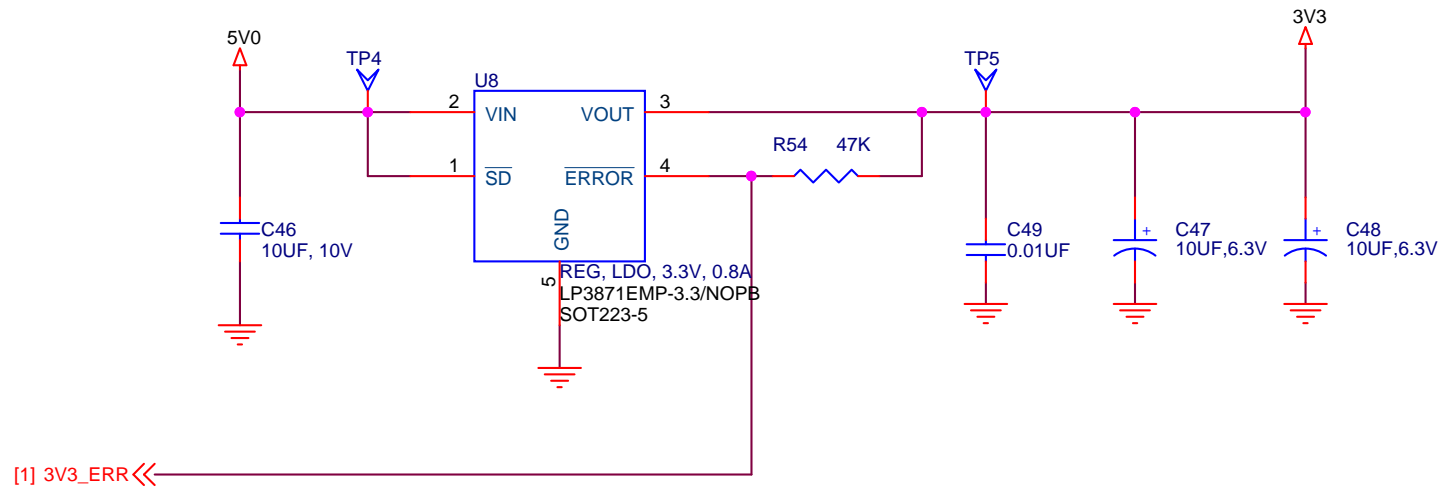
[1,5,6] RSPCK-A

[1,5] MISO-A

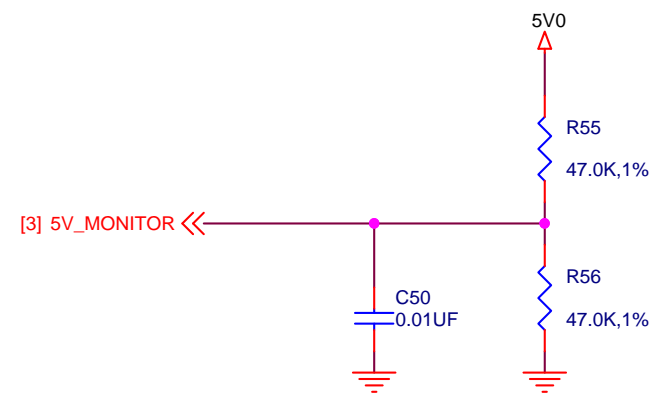


MICRO SD SOCKET

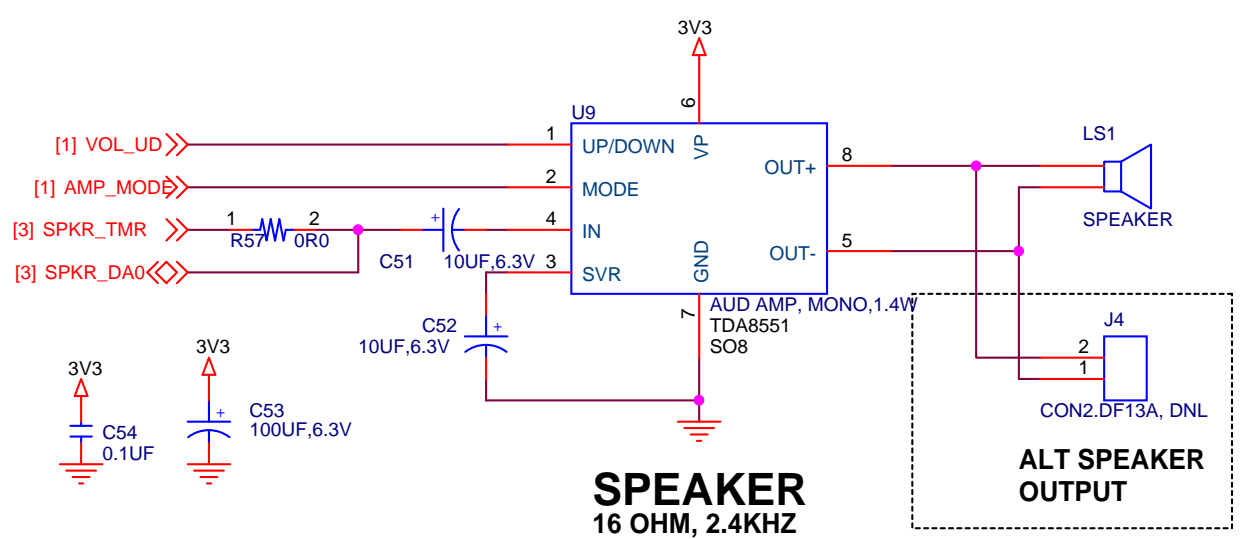
FUTURE DESIGNS, INC. 2702 TRIANA BLVD HUNTSVILLE, AL 35805		FDI
Title uEZGUI-RX 3.5"		
Size A	Document Number <Doc>	Rev 2unrel
Date:	Wednesday, October 19, 2011	Sheet 4 of 6



3.3V REGULATOR, 0.8A

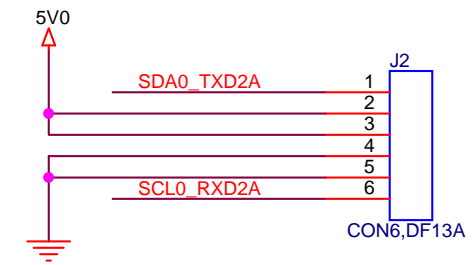
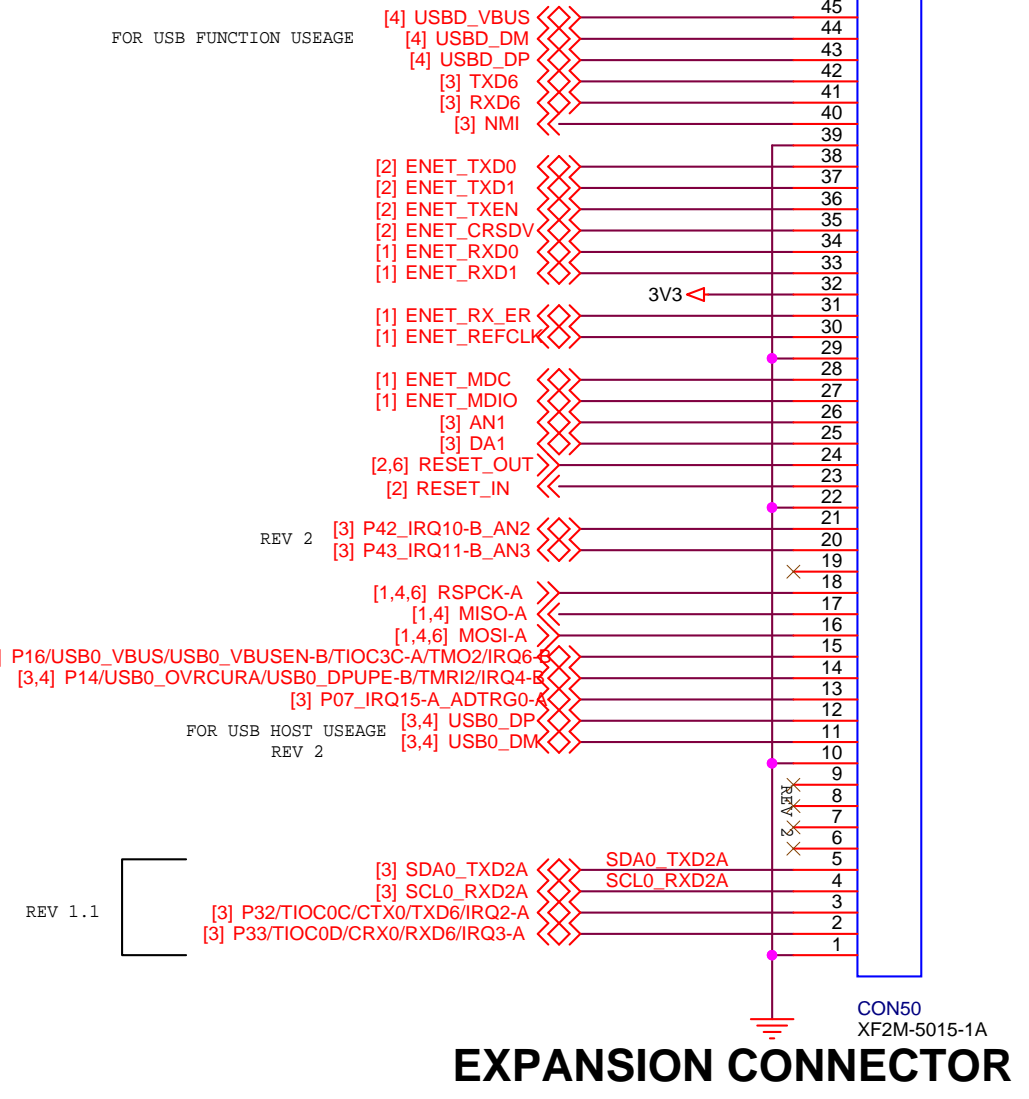
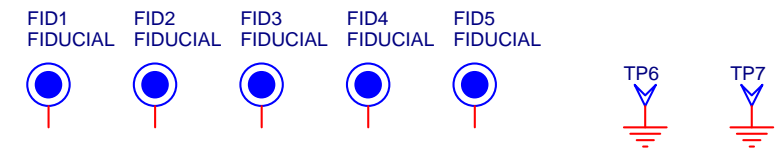


5V INPUT MONITOR VIA ADC



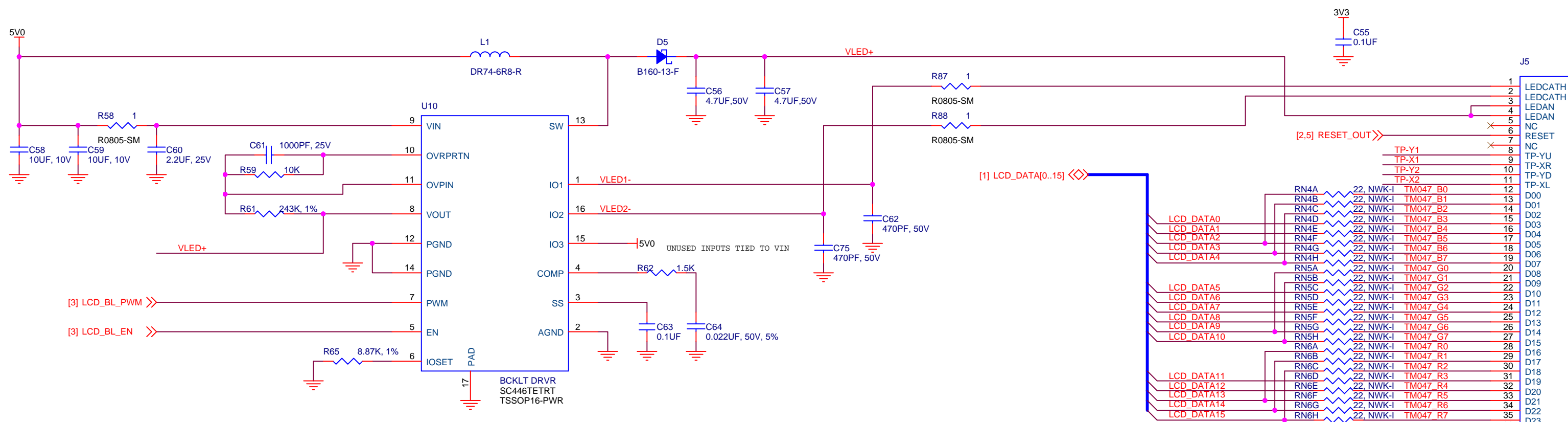
**SPEAKER
16 OHM, 2.4KHZ**

**ALT SPEAKER
OUTPUT**

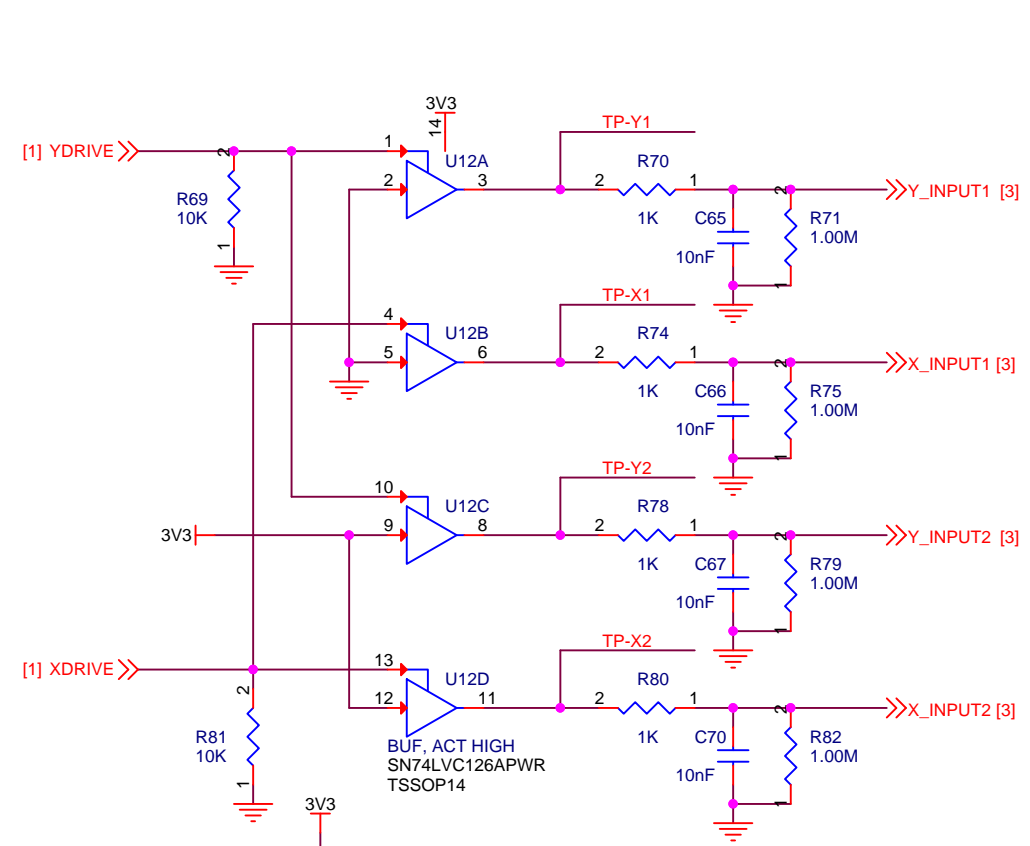


**ALTERNATE POWER &
COMM INTERFACE**

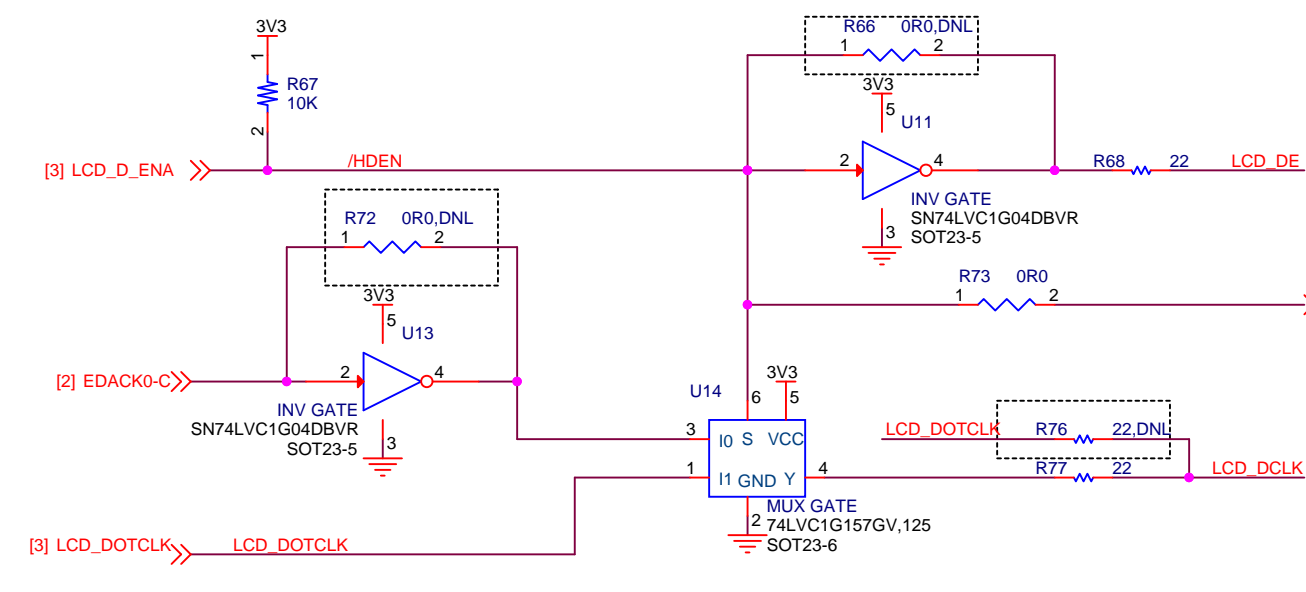
FUTURE DESIGNS, INC. 2702 TRIANA BLVD HUNTSVILLE, AL 35805		FDI
Title	uEZGUI-RX 3.5"	
Size	B	Rev
Document Number	<Doc>	2unrel
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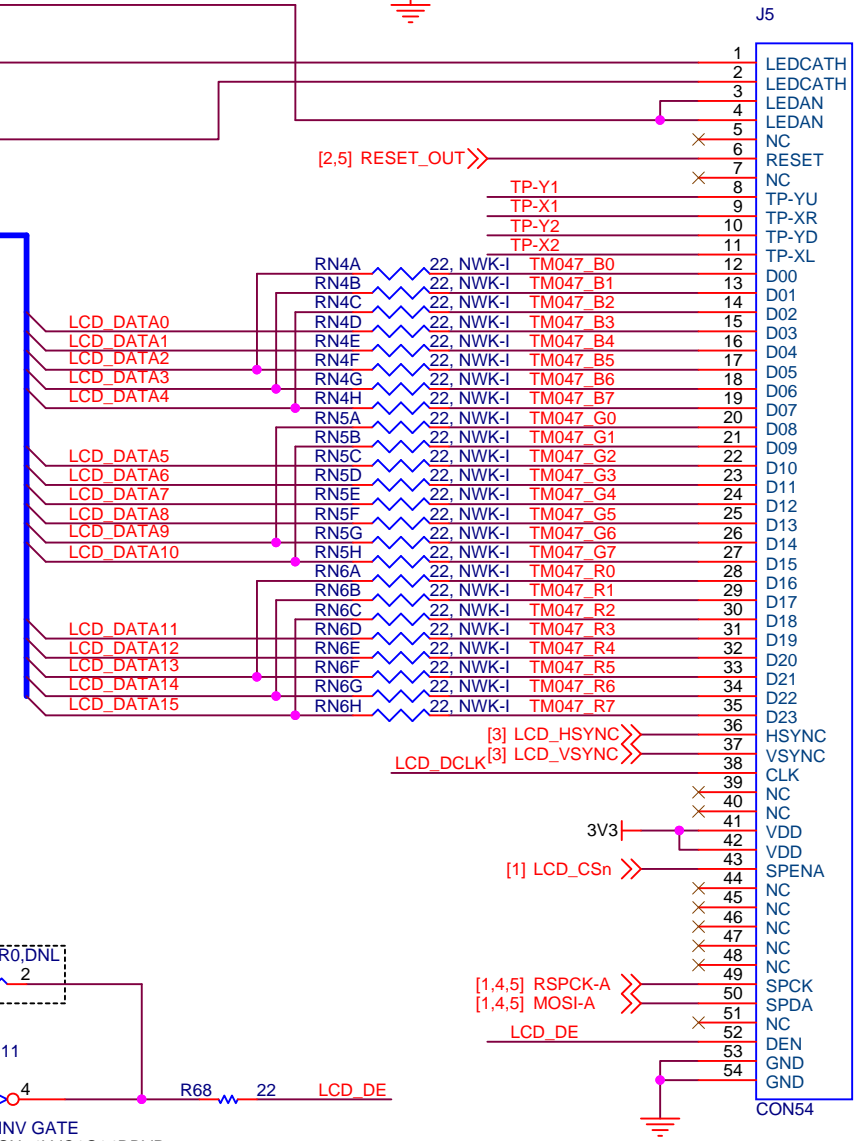
BACKLIGHT GENERATOR



TOUCH PANEL LOGIC



DD 'GLUE' LOGIC



LCD1
LCD, TIANMA 3.5"

FUTURE DESIGNS, INC. 2702 TRIANA BLVD HUNTSVILLE, AL 35805		FDI
Title	uEZGUI-RX 3.5"	
Size	Document Number	Rev
Date:	Friday, October 28, 2011	Sheet 6 of 6