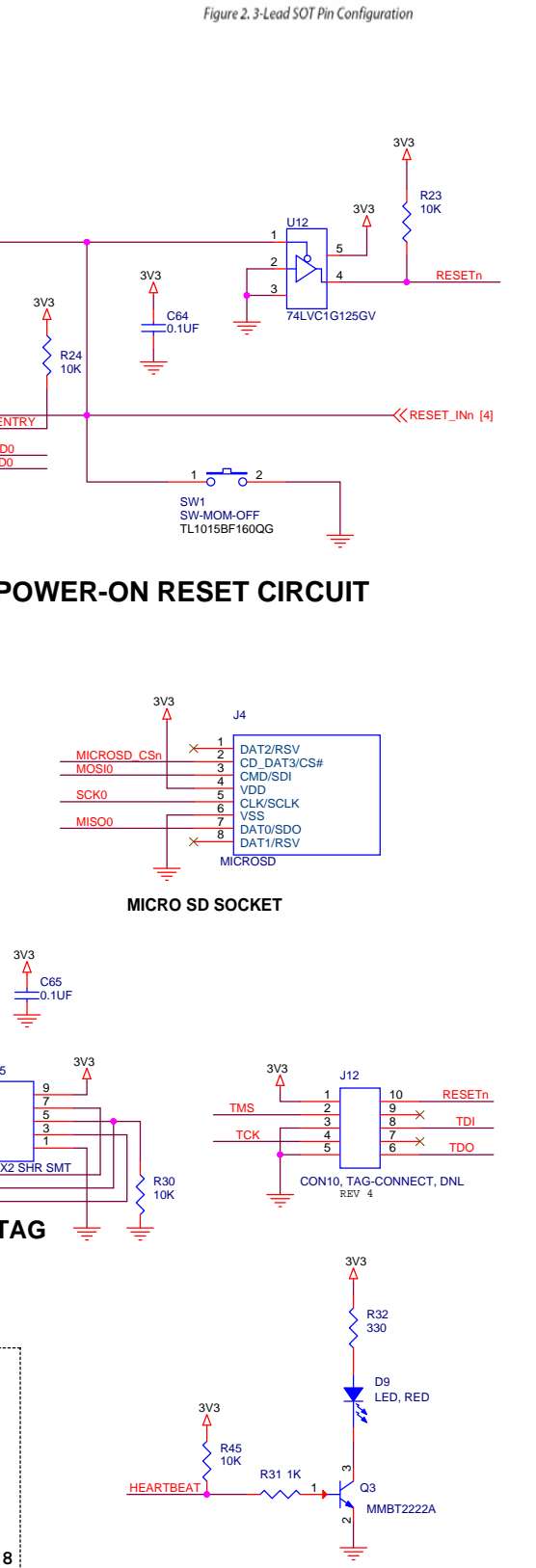
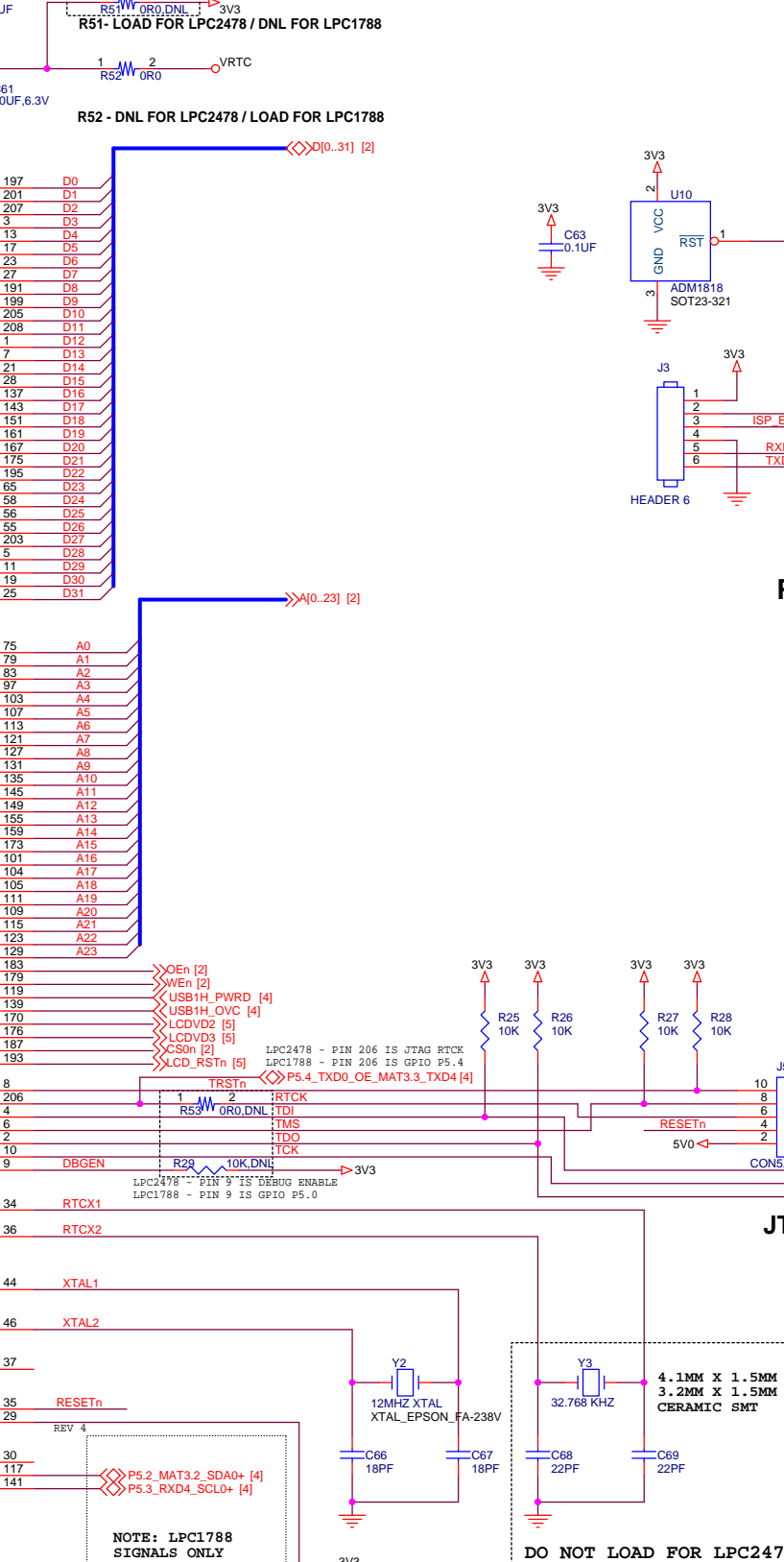
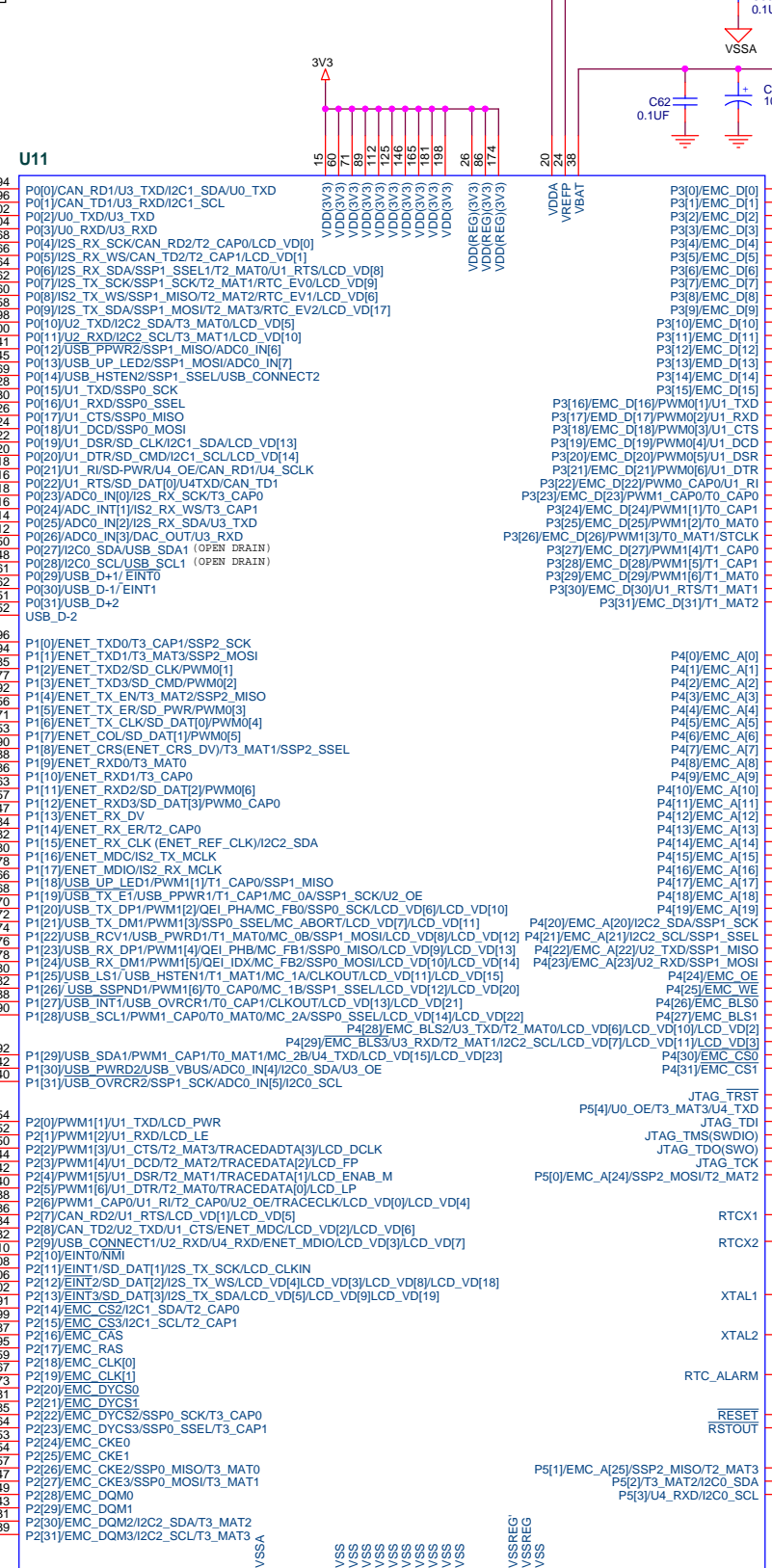
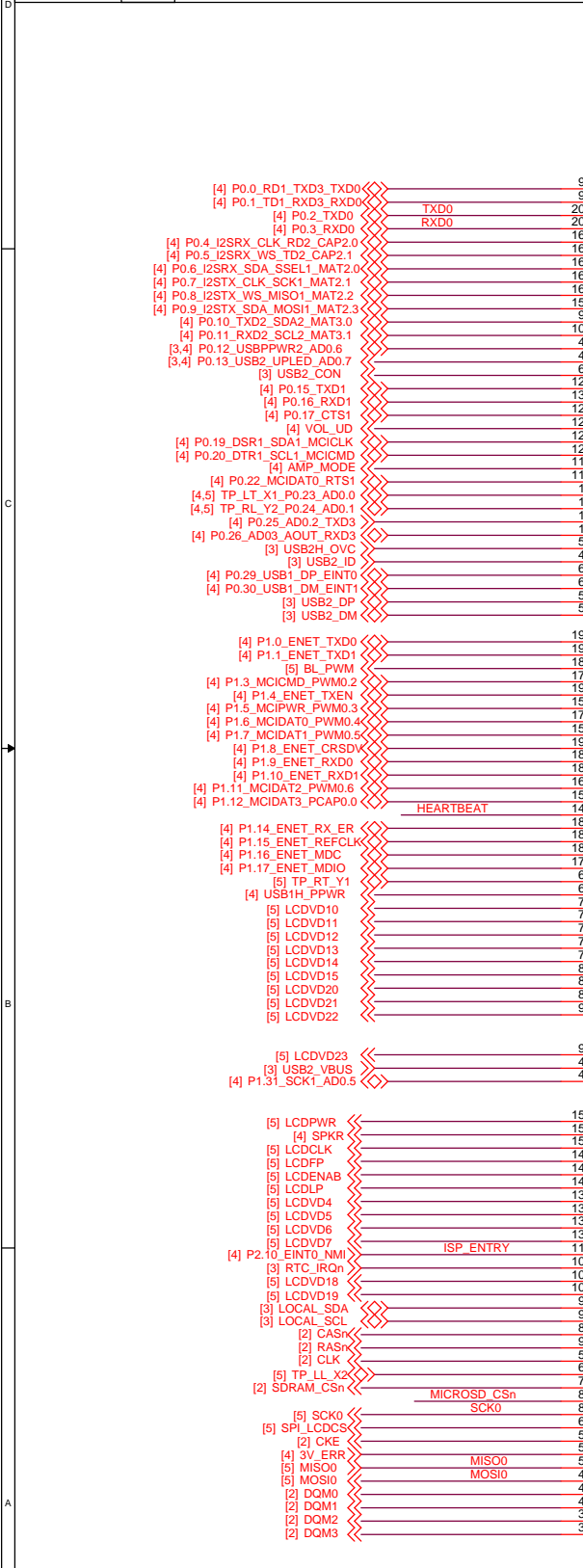


REVISION HISTORY		
01/27/10	1	INITIAL RELEASE
5/3/10	1.1	MOVE SPEAKER OUTPUT, ADD CAP, REWORK SUPERCAP
5/18/10	2	INCORPORATE REWORK INTO ARTWORK AND CHANGE ACCELEROMETERS, CHANGE PWR LED TO STATUS, DNL D5, ENLARGE MTG HOLDS, RECONFIGURE AND MOVE SPKR OUTPUT
04/01/11	3	MODIFICATIONS TO SUPPORT LPC1788 & TO MORE CLOSELY MATCH THE UEBGUI7
03/08/2012	4	SPLIT RESET_OUT, ADD PCT & PWR/COMM, CHANGE BL DEFAULT TO DISABLED
5/31/2012	5	CHANGE LCD INTERFACE TO SUPPORT 'DG28' MODULE



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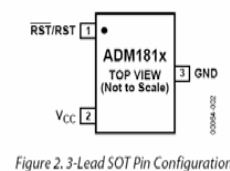


Figure 2. 3-Lead SOT Pin Configuration

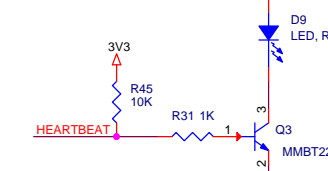
POWER-ON RESET CIRCUIT

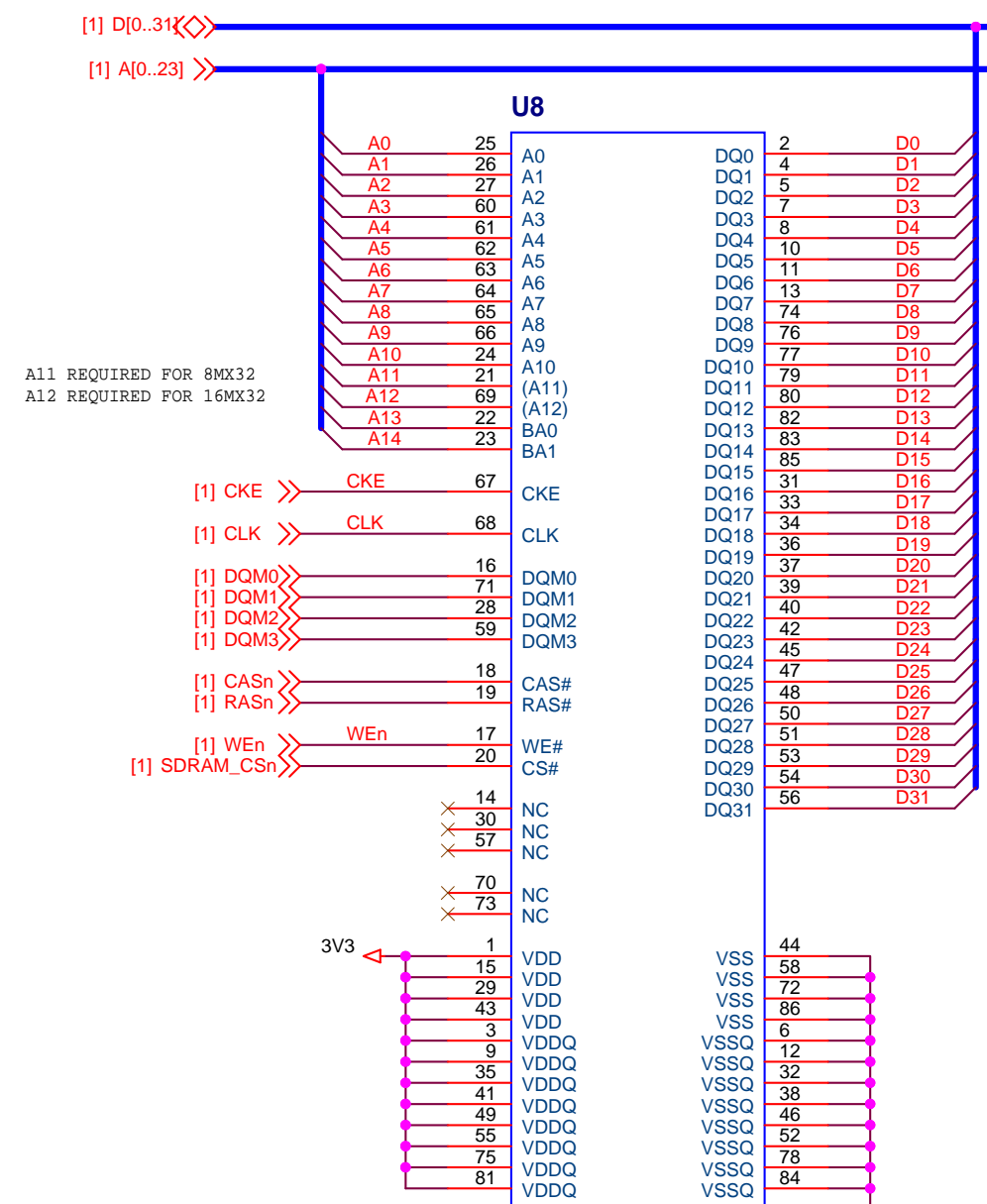
MICRO SD SOCKET

JTAG

DO NOT LOAD FOR LPC2478
LOAD FOR LPC1788

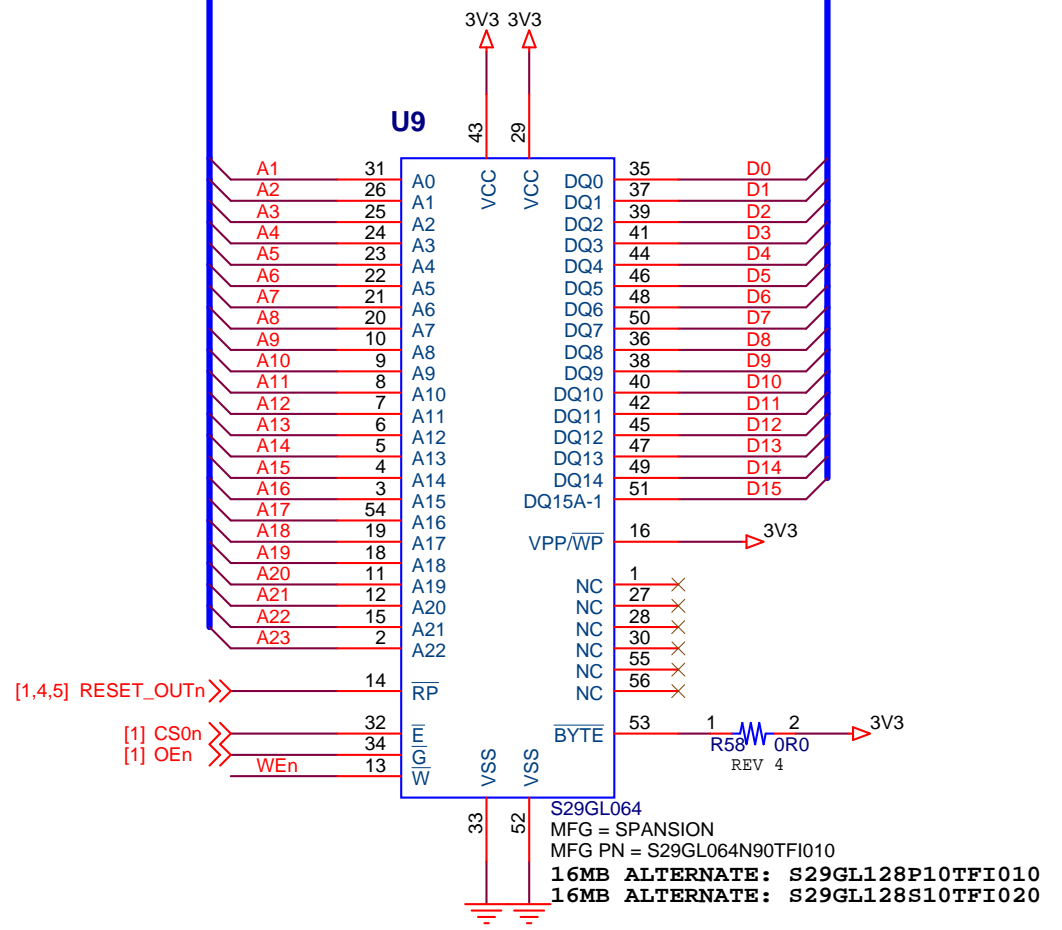
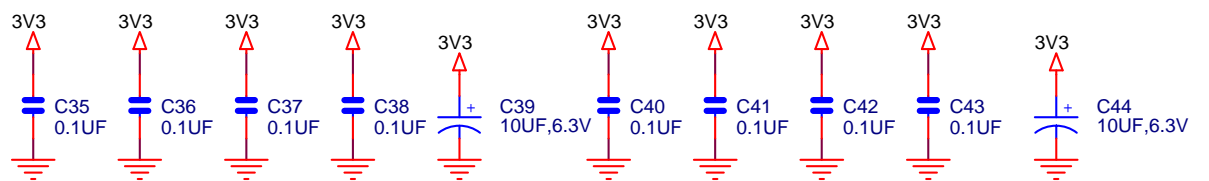
NOTE: LPC1788 SIGNALS ONLY



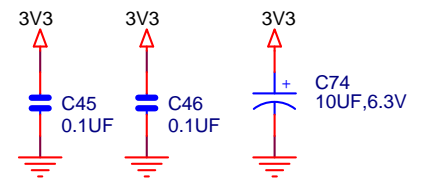


MT48LC2M32B2P
 MT48LC4M32B2P ALTERNATE (16MB)
 IS42S32800D-7TL ALTERNATE (32MB)

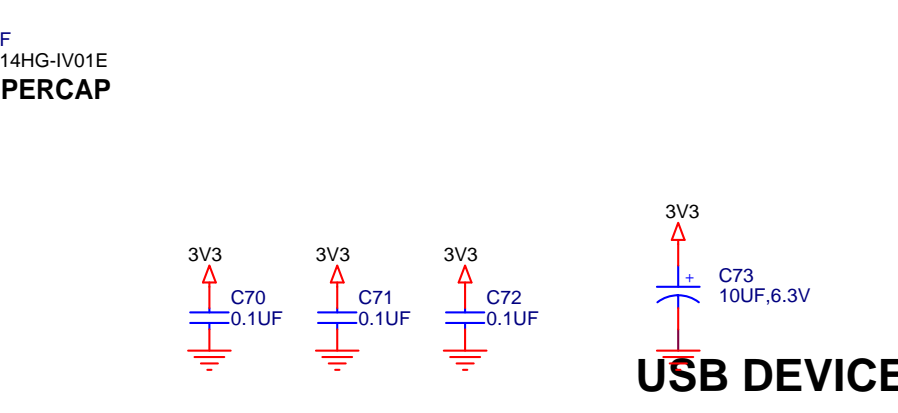
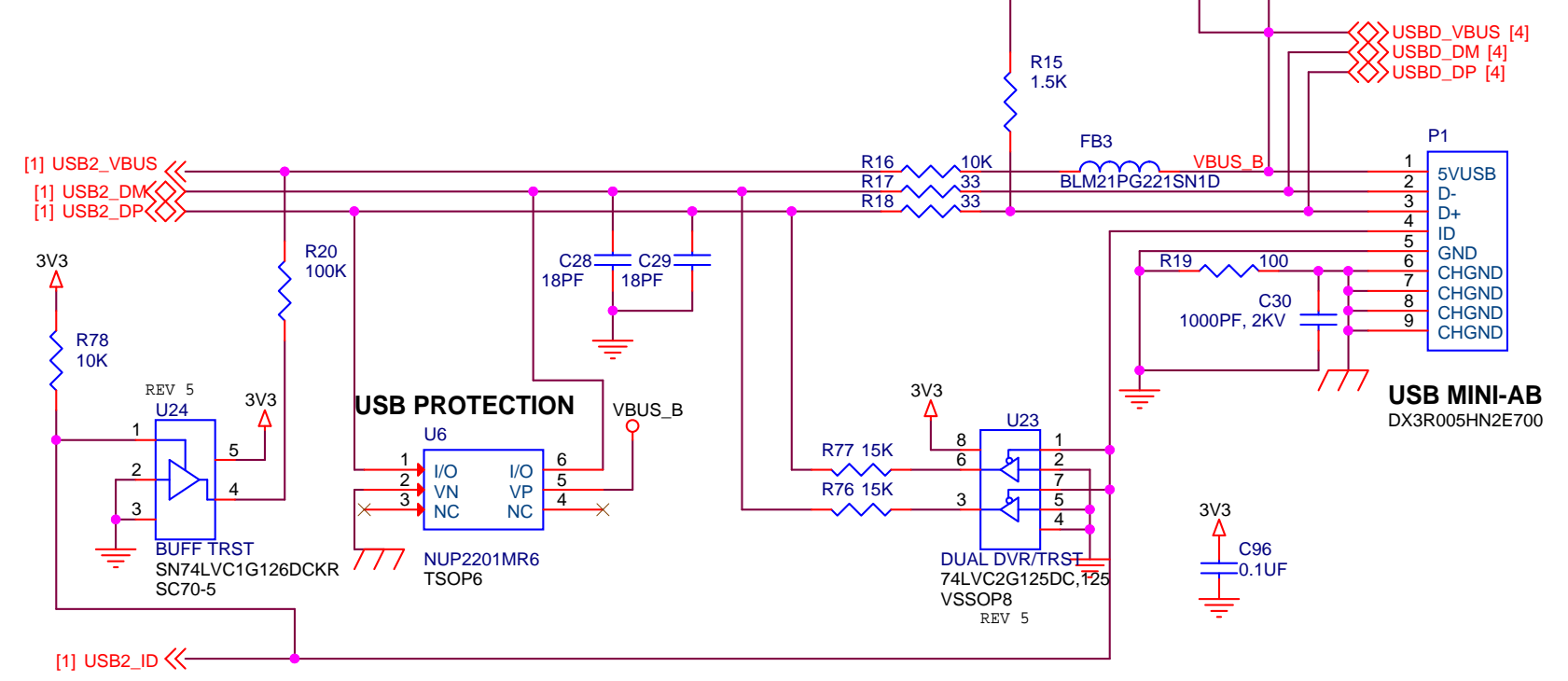
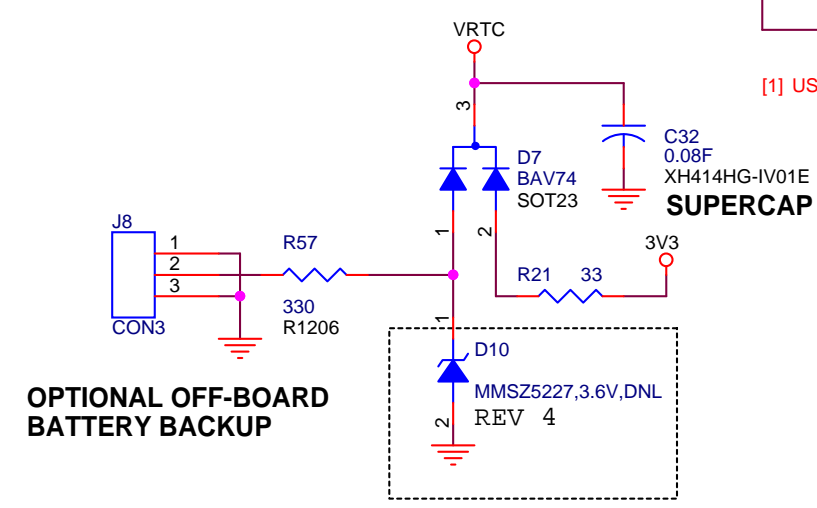
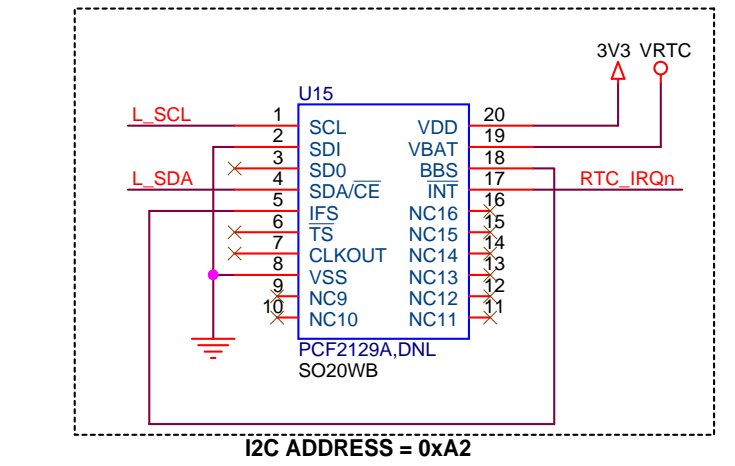
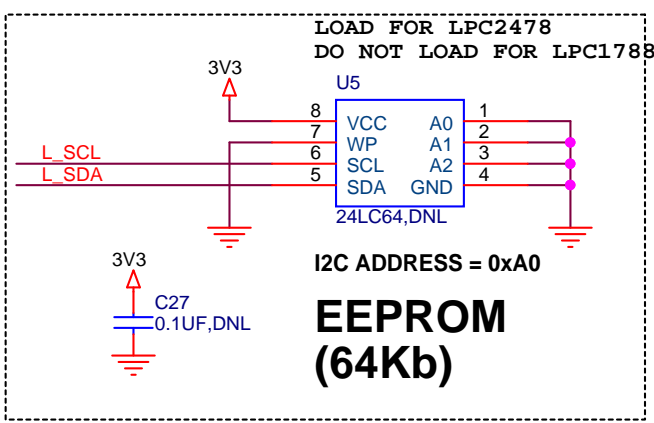
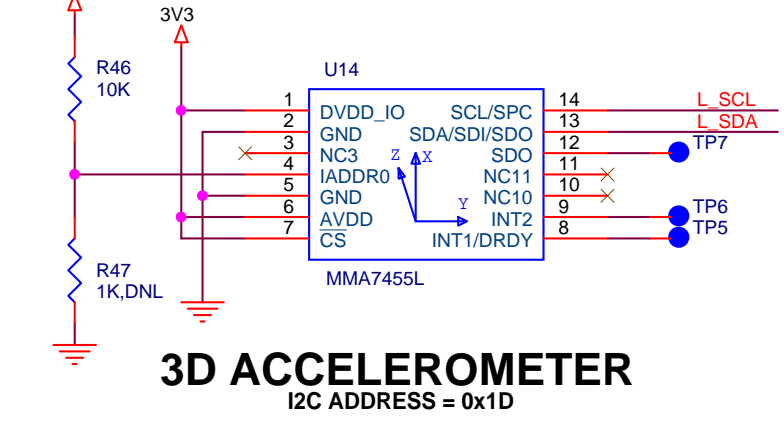
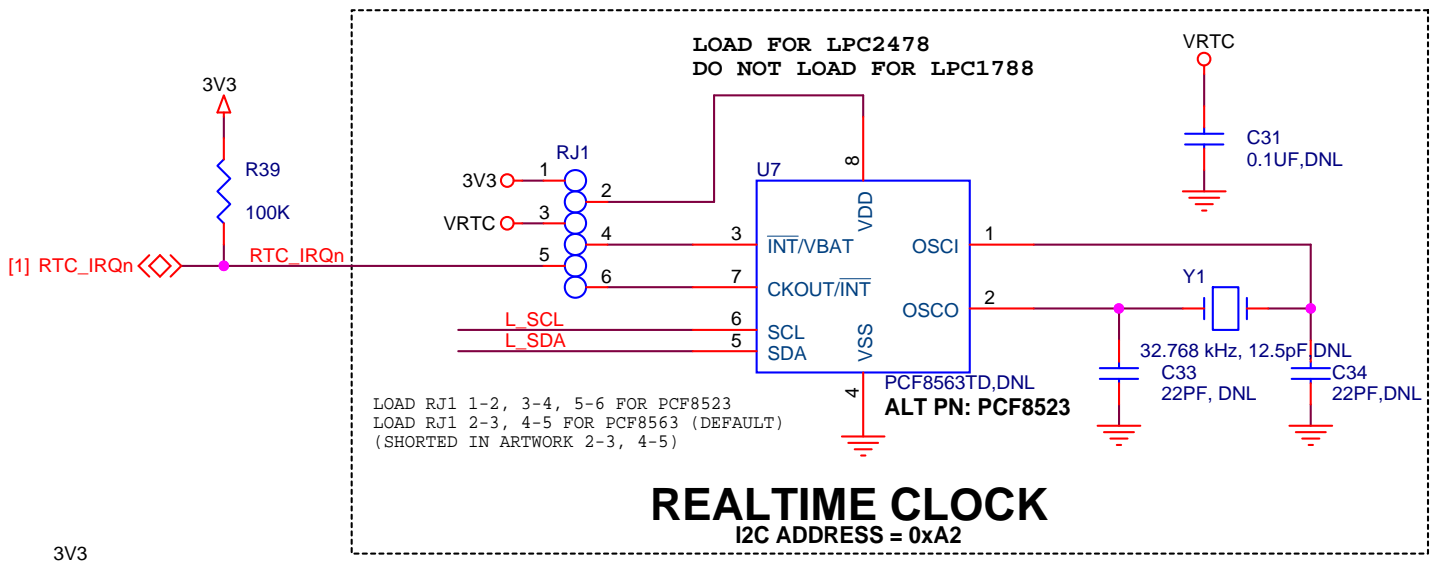
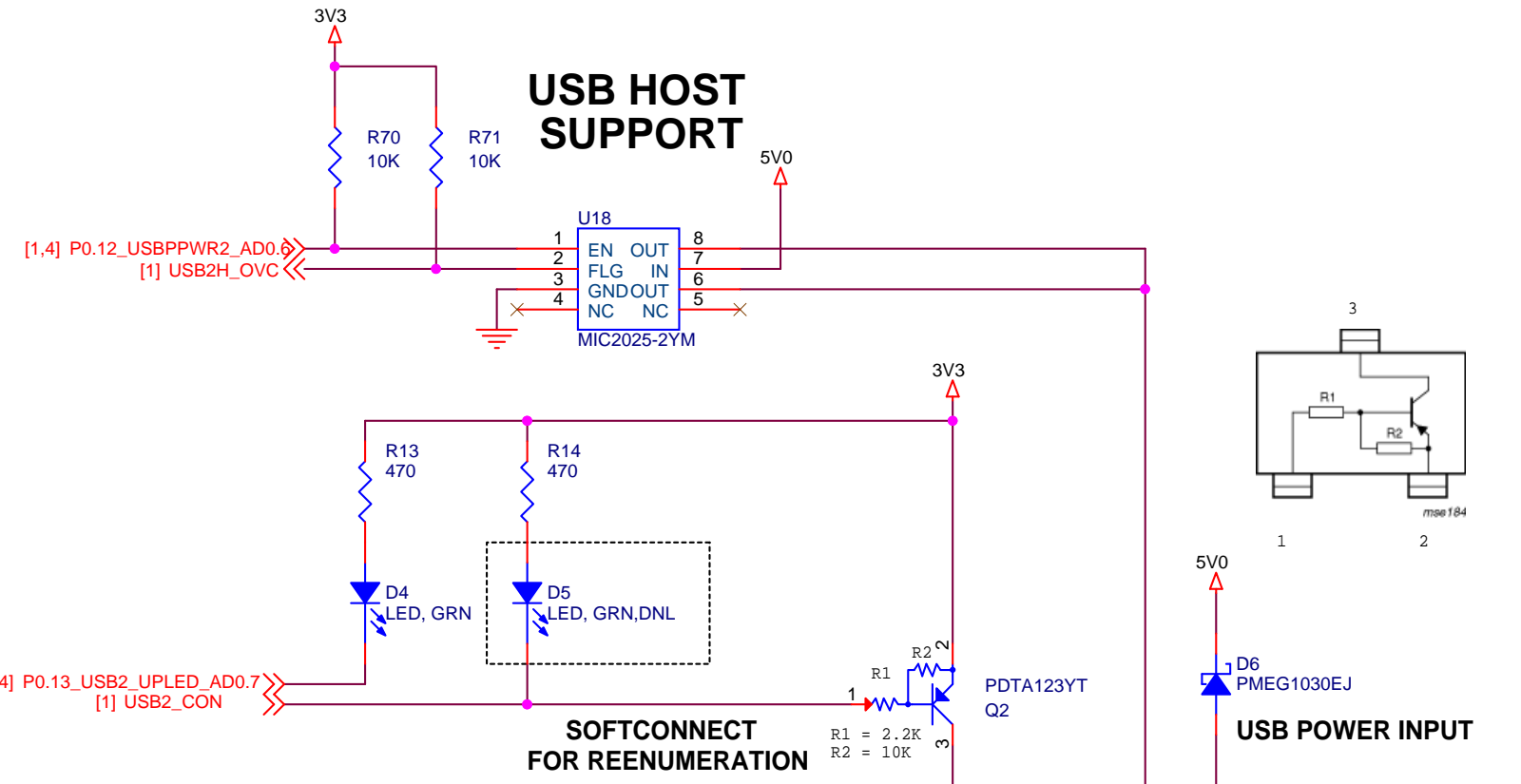
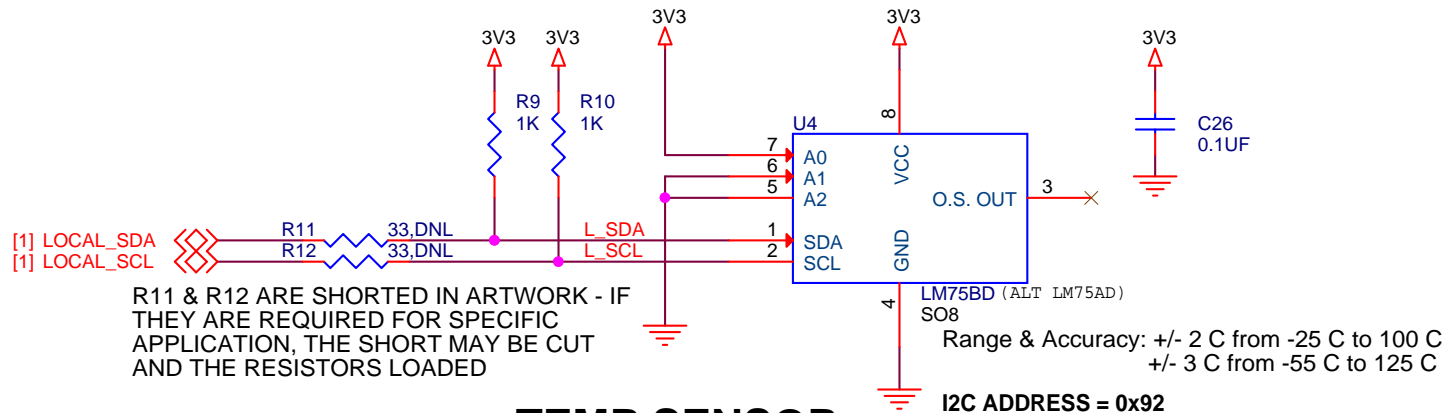
SDRAM (8MB TO 32MB)



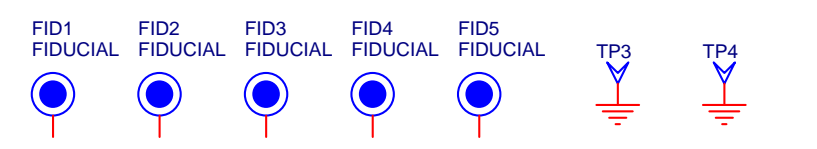
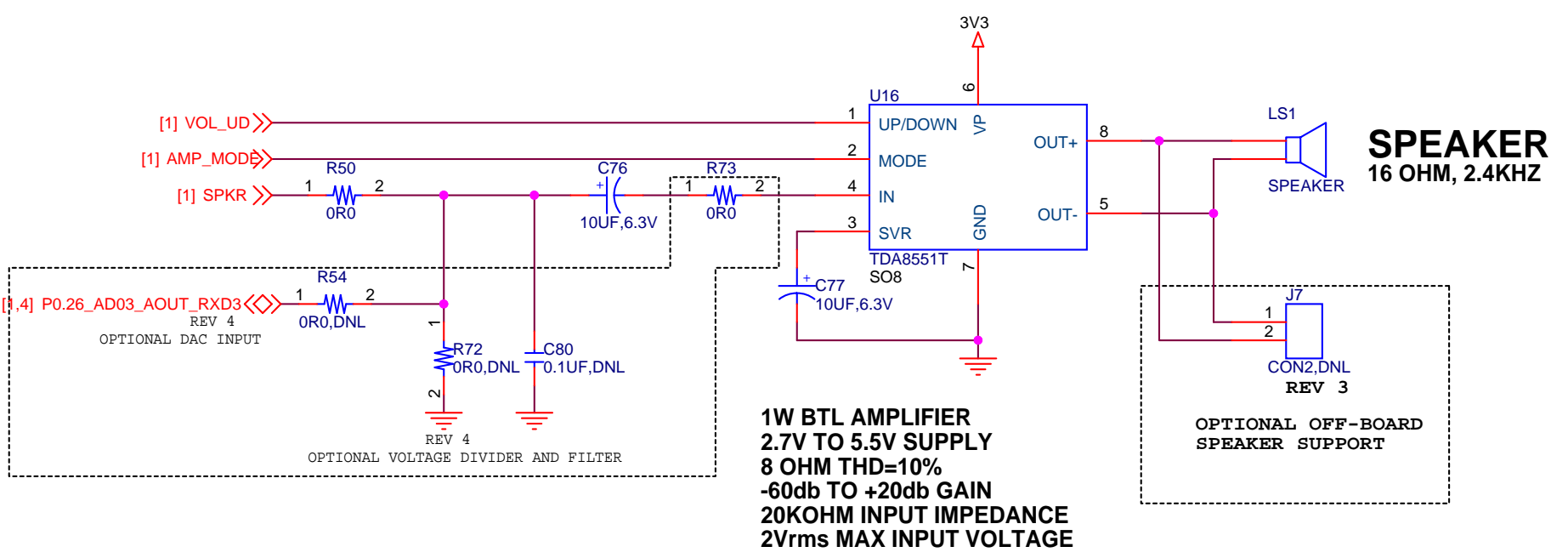
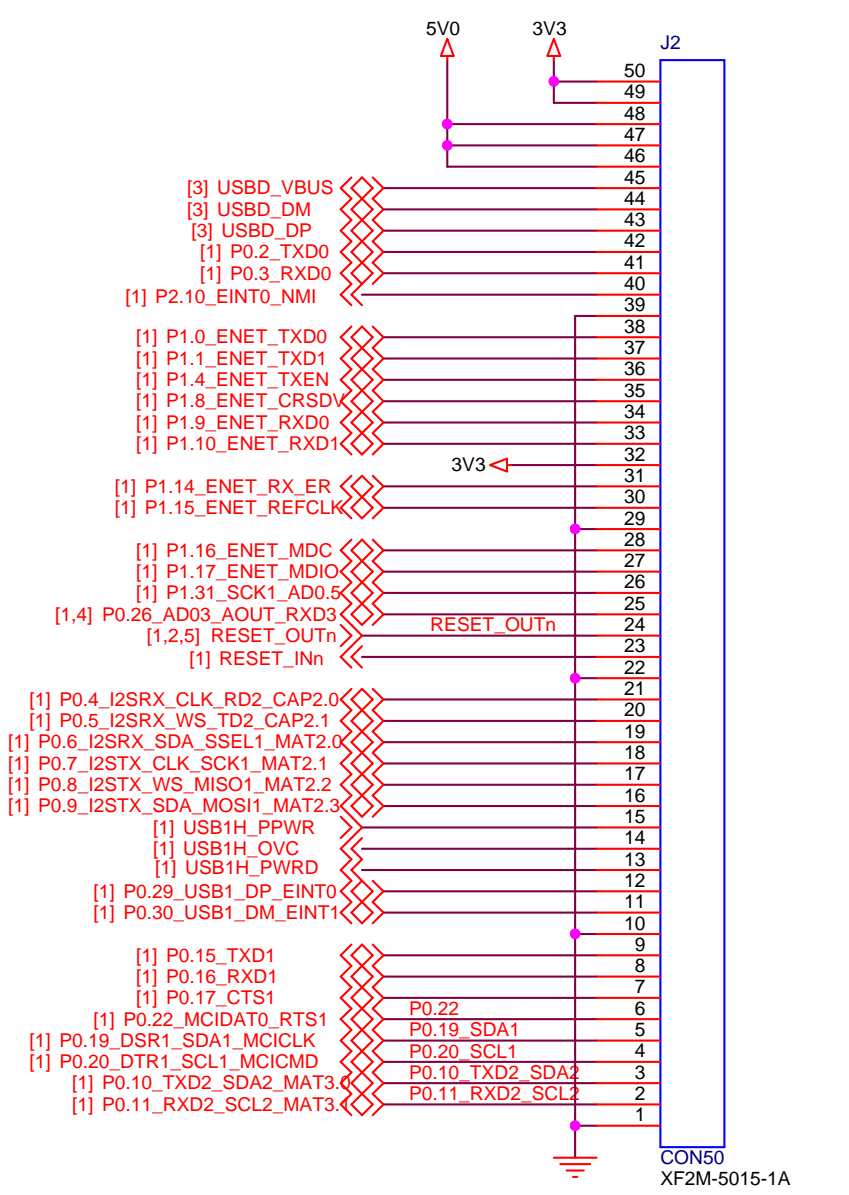
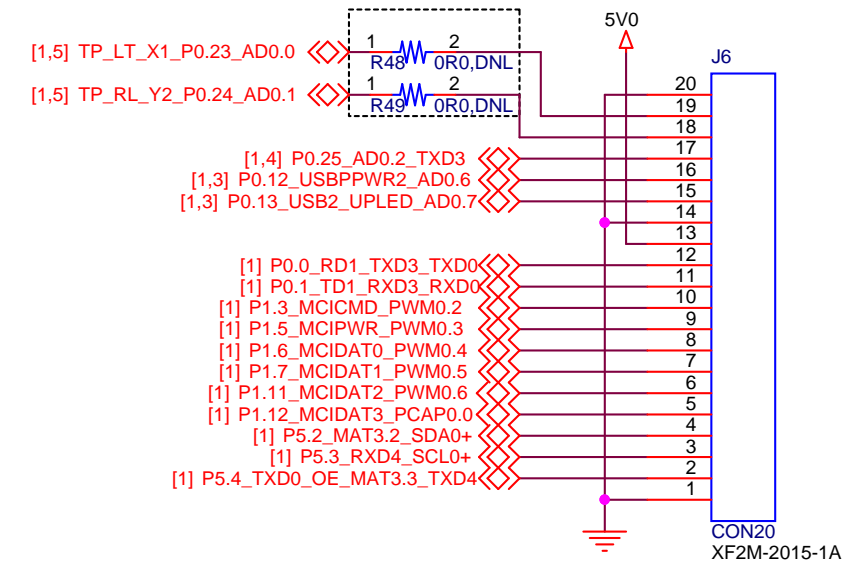
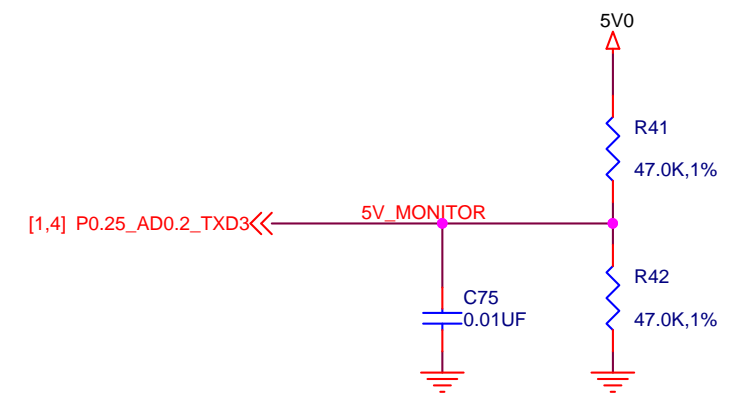
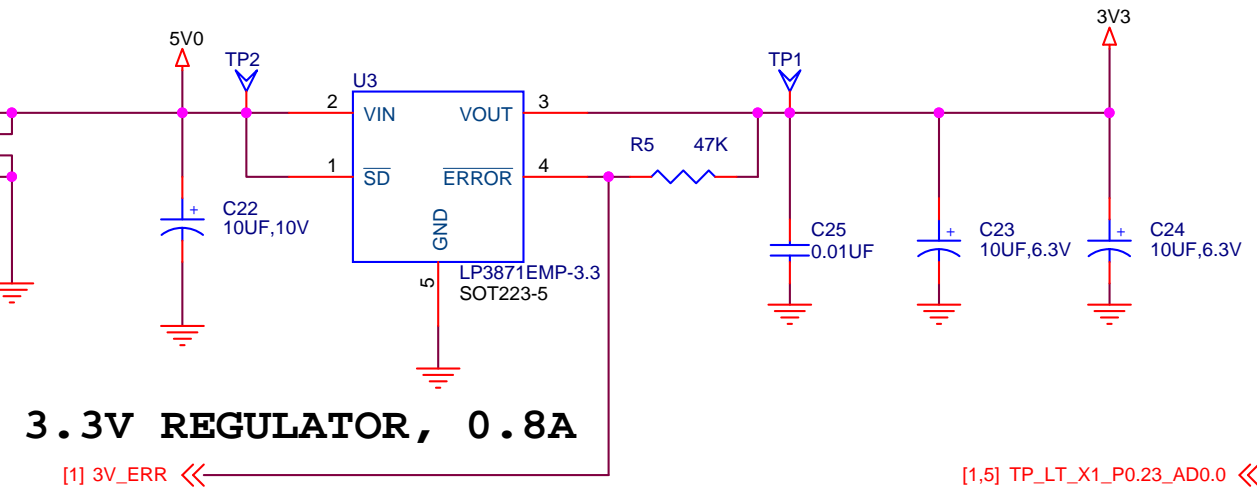
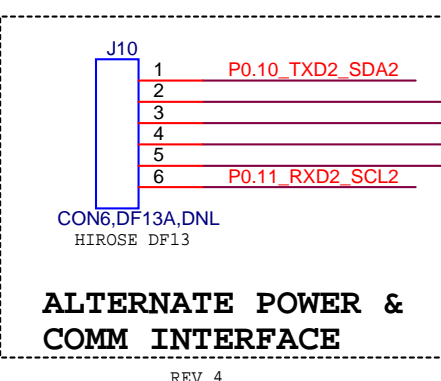
NOR FLASH (8MB TO 16MB)



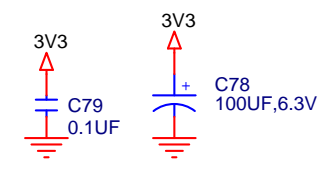
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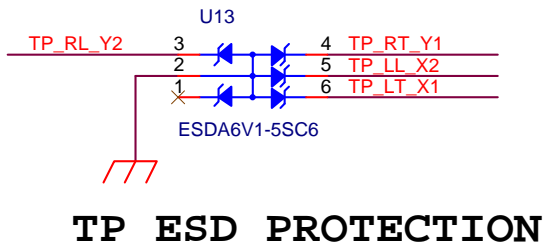
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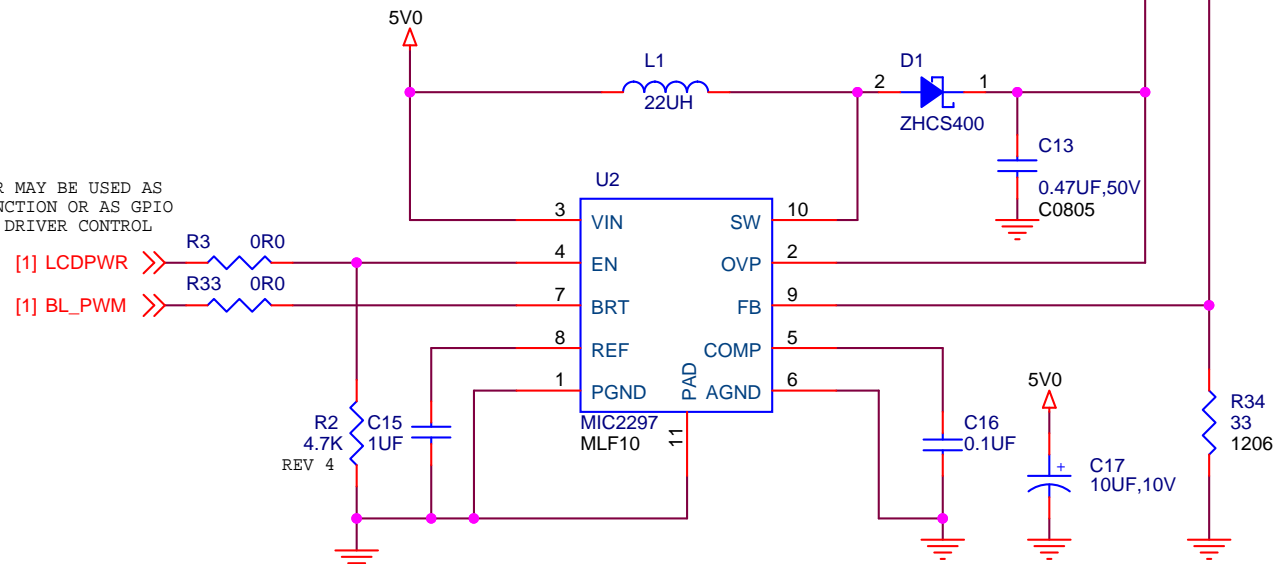


SHARP LCD



TP ESD PROTECTION

LCDPWR MAY BE USED AS HW FUNCTION OR AS GPIO UNDER DRIVER CONTROL

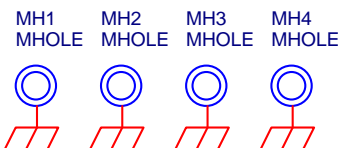


BACKLIGHT VOLTAGE GENERATOR

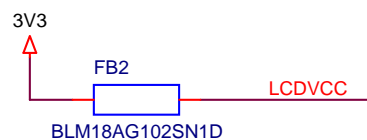
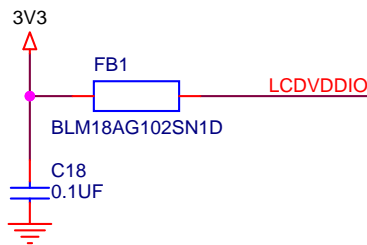
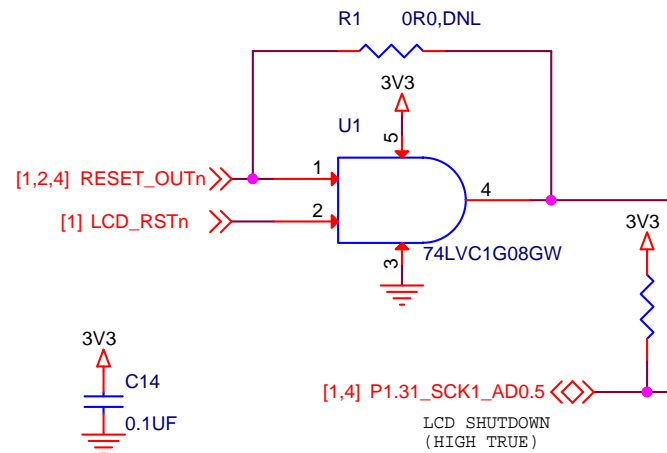
BACKLIGHT CURRENT CALCULATION:

$$I_{LED} = \frac{V_{peak} \cdot D}{5 \cdot R_{sense}}$$

I_{LED} = 20mA FOR THE FOLLOWING;
 R_{SENSE} (R34) = 33OHM
 V_{PEAK} (BRT PIN) = 3.3V
 D (BRT PIN) = 0% TO 100%

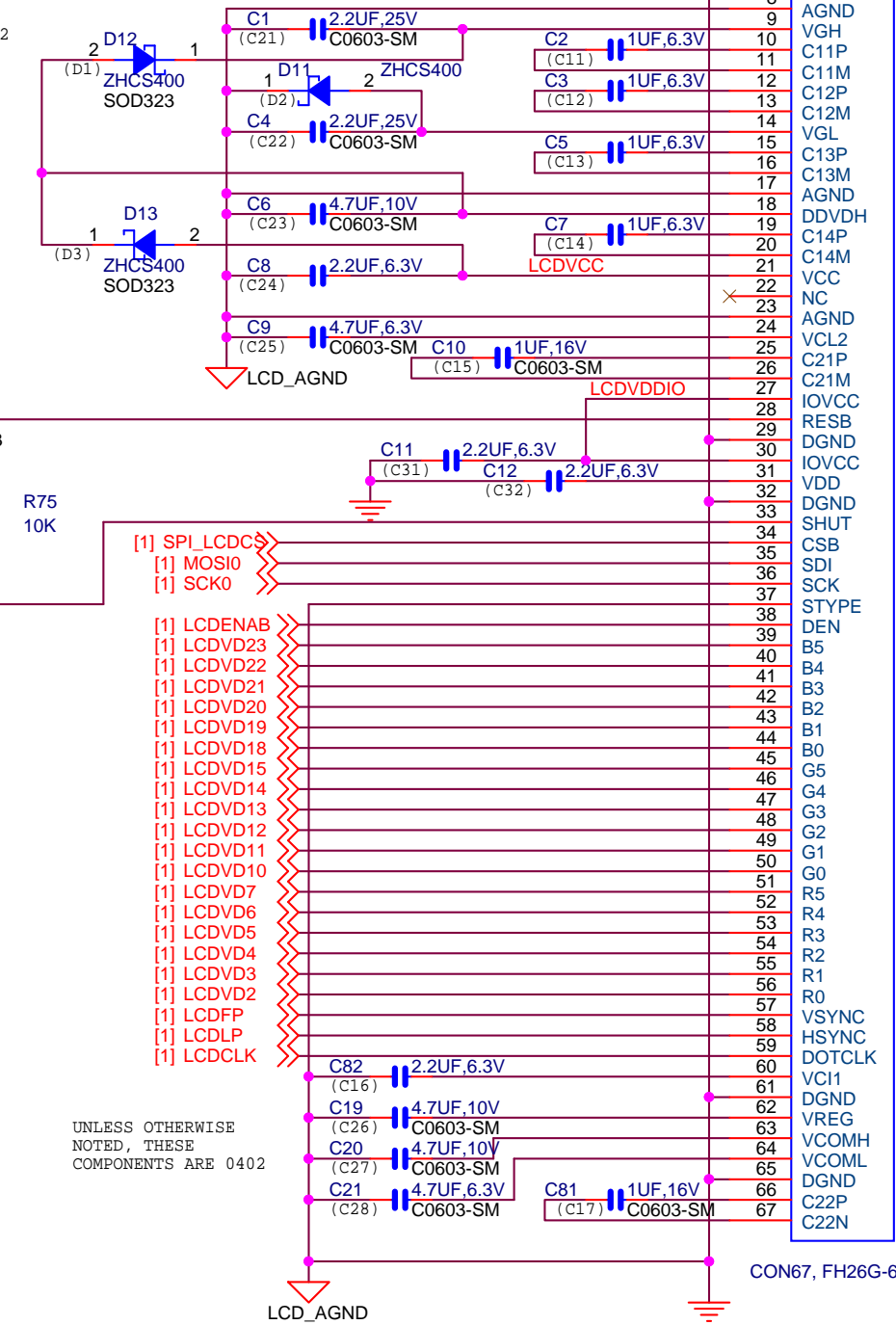


SUPPORT FOR CPU RESET CONTROL OF LCD MODULE LOAD U1 AND DNL R1



UNLESS OTHERWISE NOTED, THESE COMPONENTS ARE 0402

[1,4] TP_LT_X1_P0.23_AD0.0 TP_LT_X1
 [1,4] TP_RT_Y2_P0.24_AD0.1 TP_RT_Y2
 [1] TP_LL_X2 TP_LL_X2
 [1] TP_RT_Y1 TP_RT_Y1



CON67, FH26G-67S-0.3SHBW(05)

NOTE: SHIELD LCD_AGND AND CONNECT TO GND AT A SINGLE POINT

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