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|----------------------|---------------------------------|-------------------------|--------------------|-----------------------|--|
| FDI | ENGINEERING CHANGE ORDER | | | ECO NO: 18-005 | |
| | | | | Page 1 of 7 | |
| TITLE | CURRENT ASSY PN | CURRENT ASSY REV | NEW ASSY PN | NEW REV | |
| uEZGUI-4357-50WVN-BA | AUG4350VNBA14 | 1.4 | AUG4350VNBA20 | 2.0 | |
| uEZGUI-4357-50WVN | AUG4350VN14 | 1.5 | AUG4350VN20 | 2.0 | |

BACKGROUND:

- Update secondary expansion connector to provide QEI signal and add QEI function name to pin labels
- Update design to properly support resistive touch LCD
- Update power supply system to include dedicated USB socket for power input, change to 3A capable DCDC, and add input protection diode
- Add pullup to LCD 'DISP' signal to ensure the signal is pulled 'true'
- Change SD socket power supply to default power on
- Add XBee Socket – no module loaded
- Add optional Security ICs and external very low power RTC
- Add optional Vertical Pmod Socket
- Add GPIO controlled reset capability for Pmod socket
- Shift MCU ADC supply filter circuit slightly away from MCU to clear the body of the MCU
- Change SDRAM to I-temp version for extended temperature support
- Update components to condense BOM common part numbers

DESCRIPTION OF CHANGE:

- Change pin 3 of J5 from GPIO6.29/CTOUT8 to GPIO4.10/QEI_PHA

REV 2 [2] GPIO4.10/QEI_PHA

- Add QEI function name to pin labels for pins 11 & 12 of J5 – shown below

REV 2 [2] GPIO4.8/QEI_IDX/TXD2

REV 2 [2] GPIO4.9/QEI_PHB/RXD2

- Move 4WRTP signals from ADC-only pins (U1 pin B3 & A5) to pins supporting GPIO & ADC function (U1 pin D6 & B7)

J9 pin 38 to U1 pin D6 - GPIO7.23/ADC1.2

J9 pin 39 to U1 pin B7 - GPIO7.21/ADC1.7

PF_7/U3_BAUD/SSP1_MOSI/TRACEDATA[2]/GPIO7[21]/I2S1_TX_WS/ADC1_7

PF_8/U0_UCLK/CTIN_2/TRACEDATA[3]/GPIO7[22]/ADC0_2

PF_9/U0_DIR/CTOUT_1/GPIO7[23]/ADC1_2

B7

E6

D6

A3

GPIO7.21/ADC1.7 [7] REV 2

GPIO7.22/ADC0.2/U0_CLK/CTIN2

GPIO7.23/ADC1.2 [7] REV 2

MCU U1

REV 2 [3] GPIO7.21/ADC1.7

REV 2 [3] GPIO7.23/ADC1.2

TS_YD

TS_XL

TS_YU

38

39

40

YD

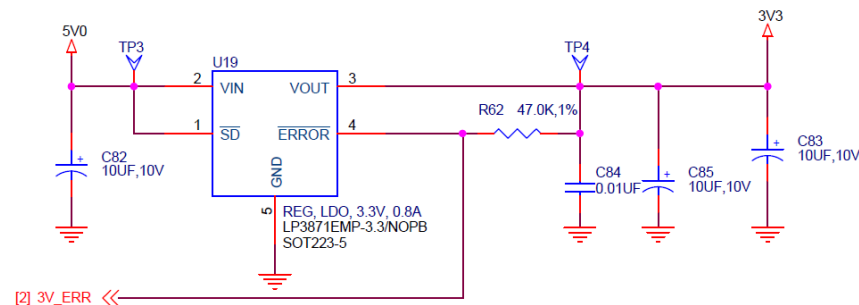
XL

LCD Connector J9

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| | | | Use as is | x |
| | | | Rework to ECO | |
| | | | Scrap & Rebuild | |
| | | | Record Change Only | x |
| Prepared by: | MH | Date: | 6/19/18 | |
| Approved by: | TE | Date: | 6/26/18 | |
| Approved by: | CM | Date: | 06/26/18 | |
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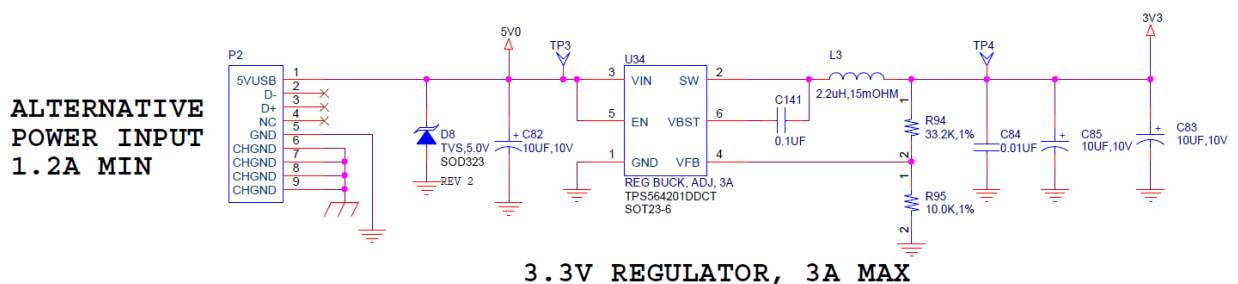
- Change 3.3V DCDC from LDO to high-capacity switching DCDC IC;
Remove U19 LP3871 U500385 and R62 47.0K R500524, delete '3V_ERR' signal



3.3V REGULATOR, 0.8A

OLD DCDC

Add U34 TPS564201 U500678, C141 C500234, L3 L500092, R94 R500748, R95 R500060, & D8 D500190



3.3V REGULATOR, 3A MAX

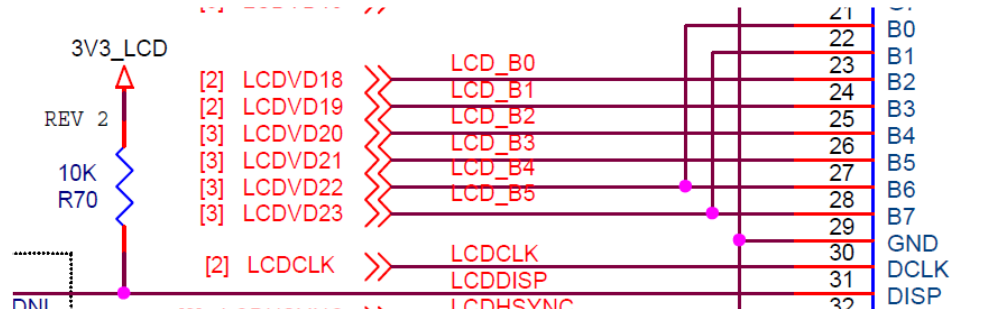
NEW DCDC

- Add 5V DC input via dedicated USB Mini-B Connector, P2, FDI PN: J500027

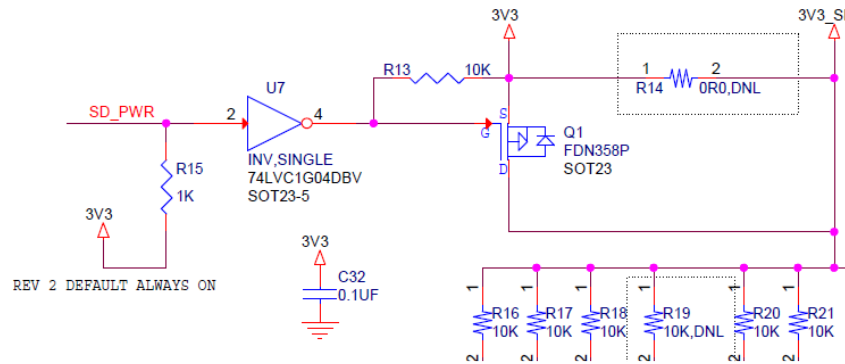
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- Add 10K ohm pullup R70 R500459 to LCD DISP signal, J9 pin 31



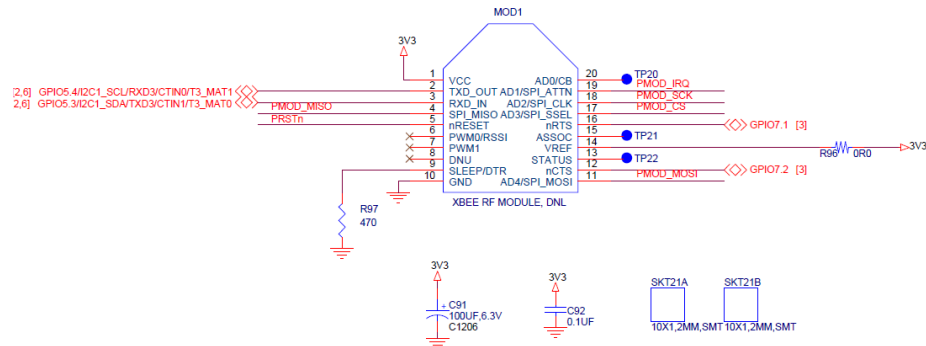
- Change SD socket power switch to default to always – change R15 from pull down to pullup;



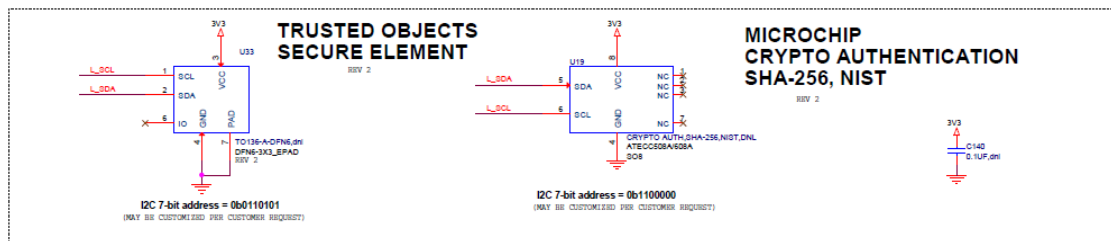
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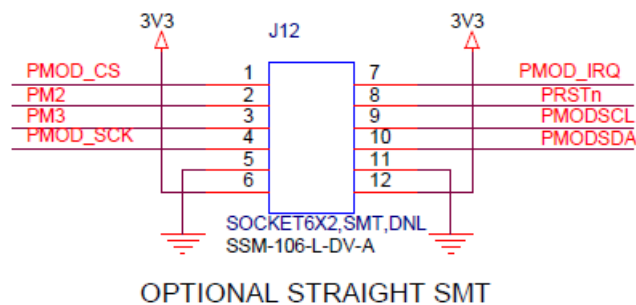
- Add XBee socket for optional wireless modules, SKT21A SK50010, SKT21B SK50010, C91 C500284, C92 C500234, R97 R500469, & R96 R500436 – no module is loaded



- Add optional security ICs, U33 Trusted Objects TO136 U500691 DNL, U19 Microchip ATECC608A U500706 DNL, & C140 C500234



- Add optional vertical Pmod socket, J500132 - DNL

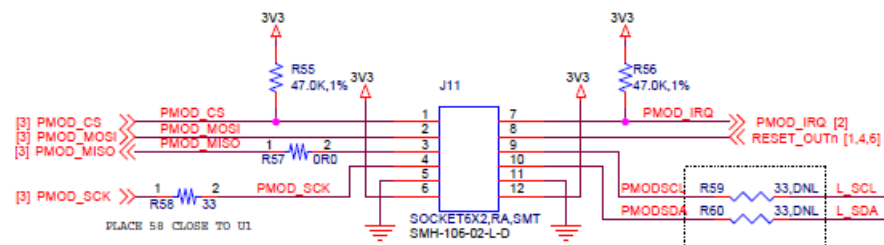


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- Add SPI/UART zero ohm resistor configuration (on J11 pin 2 & 3) and GPIO controlled capability to generate Peripheral Reset signal (J11 pin 8) to Pmod – connect PERIPH_RSTn to MCU U1 pin P14, GPIO7.0. In addition, update the Pmod schematic symbol to illustrate the pin functions.

Add U4 74LVC1G08 U500382, C93 0.1uf C500234, R71 33ohm R500461
Change R58 from 33ohm R500461 to Zero ohm R500436

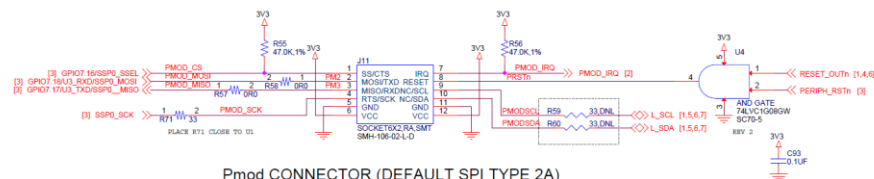


Pmod CONNECTOR (TYPE 2A)

RIGHT ANGLE SMT

NOTE: TO SUPPORT I2C;
LOAD R59/R60
DO NOT LOAD R57/R58

FROM THIS

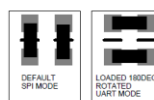


Pmod CONNECTOR (DEFAULT SPI TYPE 2A)

RIGHT ANGLE SMT

NOTE: TO SUPPORT I2C;
LOAD R59/R60
DO NOT LOAD R57/R58/R51

R57 / R58 CONFIGURATION



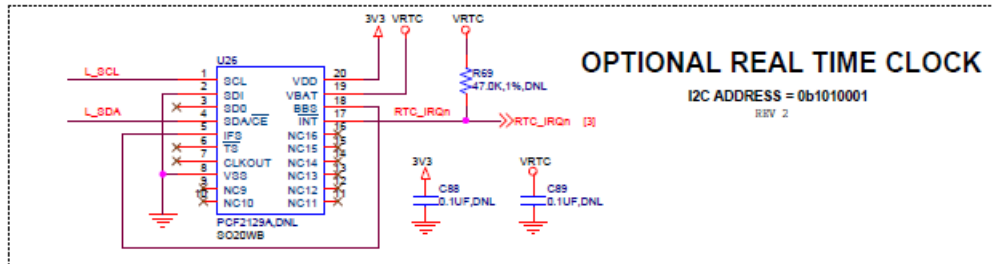
TO USE PMOD IN UART TYPE 4A:
ROTATE R57/R58 TO CONNECT RXD/TXD
PROPERLY

TO THIS

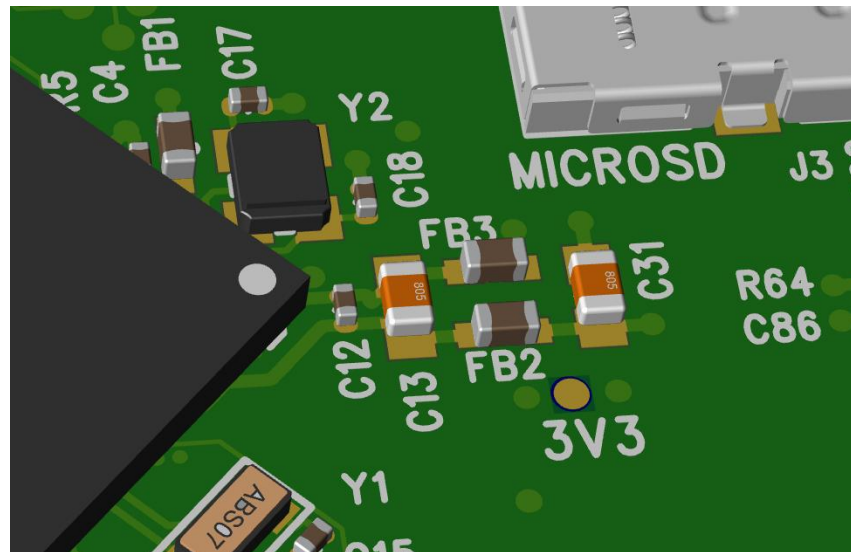
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- Add optional I2C Low Power, High accuracy Real Time Clock – U26 NXP PCF2125A U500438, R69 R500524, C88 C500234, C89 C500234, all DNL



- Shift MCU analog supply components (C12, C13, FB2, FB3, & C31) away from MCU to clear BGA package overhang – change C12 C500234 to LOAD



- Change SDRAM U8 from FDI PN U500654 Mfg PN: MT48LC4M32B2P-6A to FDI PN U500671 Mfg PN: IS42S32800J-6TLI ("I" Temp Part)
- Change C68 from C500252 10uf, 6.3V, 0805 to C500178 10uf, 10v, 0805 – remains DNL
- Change R48 from R500127 1.5K, 5% 0603 to R500522 1.5K, 5%, 0402

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REVISION INFORMATION:

| | Current Rev | New Rev |
|--|-------------|------------------------|
| uEZGUI-4357-50WVN Assembly | 1.4 | 2.0 |
| Sub-Assemblies | | |
| Mainboard Rev (AUG4350VNBA20) | 1.4 | 2.0 |
| Mainboard HW Signoff Rev | 1.4 | 2.0 |
| Schematic\BOM Rev | 1.4 | 2.0 |
| PCB Rev | 1.4 | 2.0 |
| Mainboard SW signoff Rev | 1.1 | 2.0 |
| OOB Demo | 2.09 | 2.10 Beta |
| SD Card Image | ? | Videos/Slides Only |
| FCT Software Rev | | |
| MainBoard FCT SW Rev | 1.1 | 2.0 |
| MainBoard FCT HW Rev (increase BA Rev Only when changer affects – BA_) | 1.0 | 1.0 (no new loopbacks) |
| PC FCT Application SW repository Revision | 1.00 | 2.0 |
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NOTE: FCT and Barcode Rev Changes ONLY increase the Overall Rev IF they result in the customer being able to see a difference in the product. In most cases these Rev changes will not result in an Overall Rev Change.

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